MMIC based High Power Transmit/Receive and Receive Protection Switches with integrated LNAs

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A dissertation submitted to the faculty of

Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), Gandhinagar

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), Gandhinagar

Declaration

This is to certify that

1. The thesis comprises my original work towards the degree of Doctor of Philosophy in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,
2. Due acknowledgment has been made in the text to all other material used.

Signature of Student

Certificate

This is to certify that the thesis work entitled " MMIC based high power Transmit/Receive and Receive Protection Switches with integrated LNAs " has been carried out by Ch. V. Narasimha Rao (201021009) for the degree of Doctor of Philosophy in Information and Communication Technology at this Institute under our supervision.

Prof. Deepak Ghodgaonkar
(Thesis Supervisor)

Abstract

The conventional high power microwave signal switching component is the Silicon/GaAs PIN diode, while the recently GaN pHEMT devices are being used for this application. GaAs FET, used as switching element as a PIN diode replacement, has the advantages of having fast switching speeds, simplified bias networks, monolithic compatibility, and lower power consumption driver circuitry. The major advantage of having a GaAs FET based high power T/R switch or protection switch is that other functionalities of Receiver can be integrated on to MMIC (Monolithic Microwave Integrated Circuit) making a multi-functional core-chip. However, the power performance of a FET is limited by its current-handling capability in its low-impedance state and by its breakdown voltage in its high-impedance state.

In this thesis, various new and novel circuit architectures are presented for increasing the power handling capability of GaAs FET based switches, *using low noise and low power processes*, to enable the realization of high power T/R switch with integrated LNA or absorptive high power receive protection switch with integrated LNA. So developed technique is employed for designing high power GaN FET based switches to further increase the power handling capability, beyond that of individual GaN FET switch, and also integrating LNA using the same GaN process.

On-the-chip current distributed architecture, for increasing the power handling capability, is proposed, analyzed and employed for realizing a **GaAs MMIC 10W T/R switch with integrated LNA**, employing 0.25-μm GaAs pHEMT process (PH25 of M/s UMS, France). The measured transmit loss, Noise Figure (NF) and receive path gain are 1.0 dB, 2.5 dB and 5.6 dB respectively over 9.3-9.9 GHz.

Novel *impedance transformation along with on-the-chip current distribution technique*, for increasing the power handling capability and improving the receive path loss, is proposed, analyzed, and employed for designing a **GaN MMIC 200W T/R switch with integrated LNA**, using 0.25-μm GaN pHEMT process (GH25 of M/s UMS, France). The layout level electromagnetic and co-simulation results of this 200W pulsed power handling capability T/R switch with integrated LNA are 0.8 dB transmit path loss with 45 dB receive isolation, and 2.6 dB NF with 20 dB gain for the receive path over 3.1-3.3 GHz.

Also, in this thesis, novel *FET stacking along with on-the-chip current distributed architecture,* for increasing the power handling capability and improving the receive

path loss, is proposed, analyzed and employed for realizing a **GaAs MMIC 20W absorptive receive protection switch with integrated LNA**, employing 0.13-µm GaAs pHEMT process (D01PHS of M/s OMMIC, France). The measured results are protection up to 20W with 28 dB receive isolation, 2.9 dB NF and gain of 20 dB over 9.3-9.9 GHz.

The constituent components required for designing T/R Switch with LNA, viz., high power quadrature hybrids, high power switches, LNAs are studied and design details presented.

Various high power MMIC quadrature hybrid configurations have been studied and the design, analysis and simulation results of compact distributed *high power MMIC spiral hybrid* and *high power MMIC quasi lumped impedance transforming hybrid* are presented.

MMIC GaAs and GaN HEMT based switch configurations have been studied vis-a-vis the power handling capability and novel techniques like *on-the-chip current distributed architecture* for increasing the power handling capability and *techniques of impedance transformation and FET stacking techniques* for improving the receive path insertion loss are proposed, analyzed and simulation results are presented.

MMIC GaAs HEMT based Low Noise Amplifiers' configurations have been studied and X-band single stage and two-stage LNA design, simulations and measurement results are presented. MMIC GaN HEMT based S-band Low Noise Amplifier design and simulation results are presented.

Acknowledgements

I would like to convey my sincere gratitude to Dr. K S Dasgupta, Director, DA-IICT, who had encouraged me to take up and selected me for the Ph.D work, and also has been kind enough to review my synopsis presentation and pushing me and helping me in completing the thesis.

I am greatly indebted to my supervisor Prof. Deepak Ghodgaonkar for accepting me as a doctoral student and allowing me to join his research group. He has been a constant motivator, with unflinching belief in me, demonstrating unrelenting patience in persuading me to complete the research work, providing invaluable technical guidance without which this research could not have been possible. His leadership skill and result oriented nature have created deep impression in my mind, and will continue to inspire me for the rest of the life. He has spared many Saturday and Sunday just for my work so it is difficult to find word for such kindness. But for him, this would not have been possible.

I am highly thankful to my wife, C L Madhavi, for believing in me and pushing me to complete the research work and supporting me during the entire phase. Gratitude is due to my in-laws and my parents for their blessings, belief and support.

I am highly grateful to my colleague, Mr. Piyush Sinha. He has been an outstanding help in the entire research work.

I am also grateful to Prof. Sanjeev Gupta, who has provided continuous encouragement and mentoring, during the Research Progress and Synposis reviews. I also would like to thank, The Registrar, The Dean-AP, The Convener-PG, and all other staff who directly or indirectly helped me throughout my tenure at DA-IICT. I am indebted to administrative and technical staff members of DA-IICT who have been kind enough to advise and help me in their respective roles. My sincere gratitude extends to the staff of resource center of DA-IICT.

I am very much thankful to Shri R J Doshi and Shri Chandra Prakash, who are co-students at DA-IICT, from SAC/ISRO. I am also thankful to my colleagues at SAC, for helping me complete the research work, viz., Mr. Nitesh Sharma, Mrs. Harshita Tolani, Mr. G V Reddy and Mrs. Shruti Sinha.

Lastly, I would like to present this thesis to my mother, Ch B T Sundari, and my daughter, CVTL Manasvini.

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Chapter: 1

1.0 Introduction

Active electronically scanned array (AESA) radars are currently adopted in several fields, from the ground and naval military systems, to space-borne and ground-segment civilian applications (i.e., for airspace control), to earth observation, and so on [1]. An AESA system is composed of several elementary antennas, usually in the order of thousands, in which the beam is electronically steered in different directions (i.e., by controlling the phase and amplitude of the signal to/from each array element without requiring any mechanical movement). This is accomplished by means of a solid-state transmit (Tx)/receive (Rx) module (T/R modules) behind every single radiating element. Therefore, each antenna requires thousands of TR modules. These TR modules have to allow for phase and amplitude control of the Tx/Rx signal, path selection, efficient power amplification in the Tx mode and low-noise amplification in the Rx mode. In the past, T/R module functionalities were implemented as separate monolithic microwave integrated circuits (MMICs), and then their integration was carried out by exploiting bonding wires and hybrid passive circuits on an alumina substrate [2]. Typically, gallium arsenide (GaAs) technology was selected as the platform to realize both low-noise amplifiers (LNAs) and high power amplifiers (HPAs), even if featured by different epitaxial structures to allow high power and low noise performance. The combination of bulky and heavy ferrite circulator and protection limiter or a high power receive protection switch is used to time division duplex the common antenna element between power amplifier (PA) and low noise amplifier (LNA) paths as well as protecting the LNA during transmission. In some of the applications, the combination of ferrite circulator and protection limiter/high power receive protection switch is replaced by a high power transmit/receive (T/R) switch which does time division duplexing as well as protecting the LNA during transmission or unintentional overdrives, as shown in Fig. 1-1. In either case, the switching function requires good RF performance as the insertion loss of the switch decreases power and efficiency in the transmit path, and degrades the noise figure in the receive path.

The conventional high power microwave signal switching component is the Silicon/GaAs PIN diode, while recently GaN devices are being used for this application. When a GaAs FET is used as a switching element as a PIN diode

replacement in several applications, it has the advantages of having fast switching speeds, simplified bias networks and monolithic compatibility.

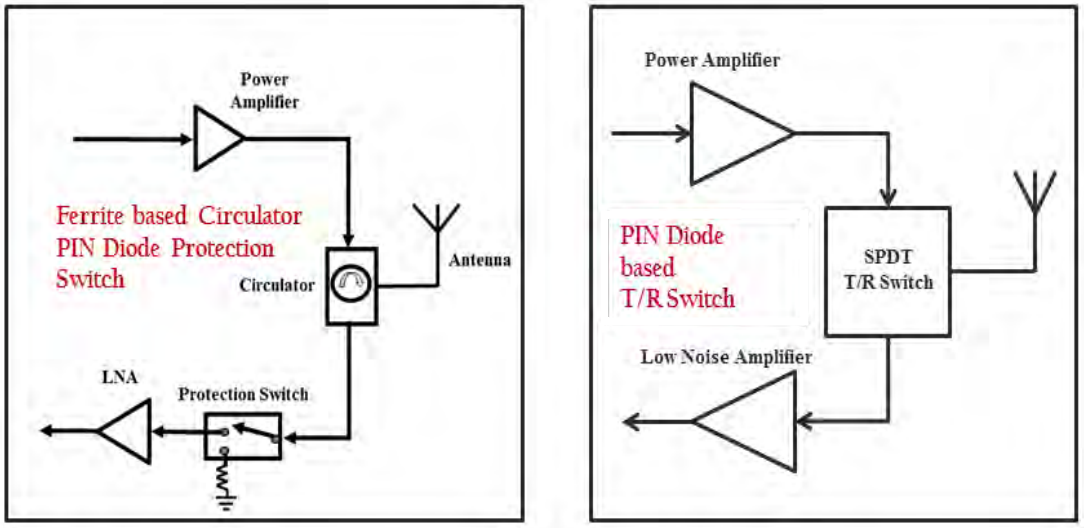

Figure 1-1. Conventional Transmit /Receive Module Front-Ends

However, the power performance of a FET is limited by its current-handling capability in its low-impedance state and by its breakdown voltage in its high-impedance state. To design high performance, high power GaAs FET T/R switches and absorptive Receive Protection switches which can handle few tens of Watts, using low power FET devices, various different circuit techniques are required to be employed. Most of the reported techniques/works were based on:

- FET Stacking technique [4], [6], wider FET employment [9], distributed shunt stacked FET technique [7], distributed terminated shunt FETs [6], distributed diode based limiter [5], [8], [10], distributed FET based limiter [10].
- Custom design of wider FETs at process level and not standard Process Design Kit (PDK) component of library provided by the GaAs Foundry.
- Power process based FETs, whose noise performance is not optimal for LNA.
- Demonstrated power handling numbers are with matched loads. Any mismatch on the output, i.e., high VSWR load, reduces the power handling capability, which could be up to 6 dB in case of open/short loads.

1.1 Motivation & Objectives

The motivation for the present work is to design GaAs FET based high power T/R switch / absorptive Receive protection switches with integrated LNAs, as a single MMIC as shown in Fig. 1-2. To accomplish this, the high power switch needs to be realized using the same process as that of a GaAs Low Noise Amplifier (LNA), which happens to be a *low power* process.

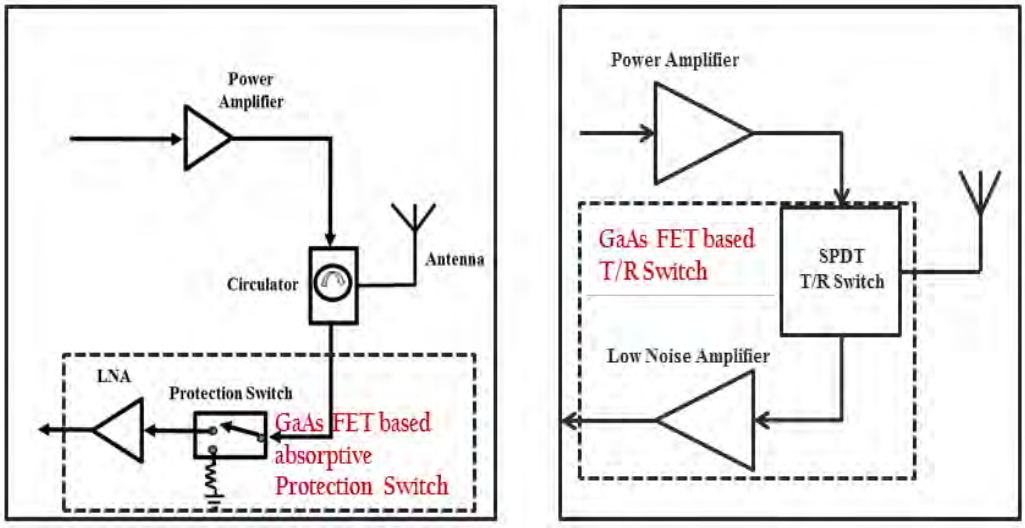

Figure 1-2. Modified Transmit /Receive Module Front-Ends

The objectives of the present research are:

- ✓ To design novel circuit architectures, other than the ones which are in vogue, to realize high power switches using low power, low noise FETs.
- ✓ To create a scalable architecture, which can be implementable on any commercially accessible MMIC foundry using their own "standard Process Design Kit (PDK)".
- ✓ To integrate LNA along with high power switch as a single MMIC
- ✓ To employ the techniques so developed, for designing high power switches using GaN FETs, beyond the capability of individual GaN FET, and integrate a GaN LNA to make a single MMIC.

The specific scope of the present research has been:

- ✓ Design, realization and characterization *of GaAs MMIC high power (10W) T/R Switch with LNA*, using a standard, commercially accessible low noise GaAs foundry process.
- ✓ Design, realization and characterization *GaAs MMIC high power (20W) absorptive Receive Protection Switch with LNA*, using a standard, commercially accessible low noise GaAs foundry process.
- ✓ Design, analysis and simulation of *GaN MMIC high power (200W) T/R Switch with LNA*, using a standard, commercially accessible GaN foundry.
- ✓ Design, analysis and simulation of all the associated circuits viz., high power quadrature hybrids, high power switch elements and LNAs using GaAs and GaN processes.

1.2 Organization of Thesis

Nine chapters of this thesis are organized as below:

Chapter:2 presents the literature survey of reported/published works with respect to various techniques employed for increasing the power handling capability of GaAs FET switches. Reported works on GaN based high power switches are also surveyed and presented.

Chapter:3 presents the design approach and analysis of various novel techniques proposed, viz., *on-the chip current distribution, impedance transformation along with on-the chip current distribution, FET stacking along with on-the chip current distribution*, along with analytical case studies for all the above case.

Chapter:4 presents the description and analysis of various types of *high power MMIC quadrature hybrids* along with the design approach, analysis and simulation of 10W and 20W MMIC compact spiral quadrature hybrids and 200W "modified" quasi lumped impedance transforming hybrid.

Chapter:5 presents the description and analysis of various types of *high power switches* along with the design approach, analysis, simulation and measurement results of 10W and 20W MMIC GaAs switches and layout level electromagnetic and co-simulation results of 200W GaN Switch.

Chapter:6 presents the description and design of LNAs along with the design approach, analysis, simulation and measurement results of X-band single-stage, X-band two-stage GaAs LNAs. Also presented is the design of and layout level electromagnetic and co-simulation results of S-band GaN LNA.

Chapter:7 presents the description, design approach, analysis, simulation and measurement results of (a) *GaAs MMIC high power (10W) T/R Switch with LNA (b) GaAs MMIC high power (20W) absorptive Receive Protection Switch with LNA* and layout level electromagnetic and co-simulation results of (c) *GaN MMIC high power (200W) T/R Switch with LNA*. The performance of these MMICs is compared with the reported works.

Chapter 8 gives the overall conclusions derived based on the different techniques presented, realized and experimentally validated results of the MMICs developed. It also gives the future scope of work as continuation to present work.

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Chapter: 2

Literature Survey

2.0 Introduction:

High power RF switches are an essential component of modern radar and communication systems which alternately connects a transmitter and a receiver to a single common antenna. Typically, T/R modules contain either a high power T/R switch or a ferrite circulator along with an absorptive high power receive protection switch for time-division duplexing. This high power switch provides low loss transmit signal path to the antenna and protects the receiver viz. low noise amplifier during transmission while ensuring a low-loss connection path between the antenna and the receiver.

Conventionally T/R modules were essentially based on passive ferrite circulators [1], [2] and PIN diodes based protection switches [4]-[7]. PIN diodes are current controlled device having high resistivity intrinsic (I) region sandwiched between p-type and n-type semiconductor The PIN diodes is used as switching element, to present either a short circuit or an open circuit, depending on the bias condition viz. its reverse and forward bias characteristics. The performance characteristics of the PIN diode depends mainly on the chip geometry and the processed semiconductor material in the intrinsic or I - region. It determines the switching speed, capacitance, breakdown voltage etc. [1]. PIN diodes can be fabricated on Si and GaAs substrate and the main benefit of PIN diode is that it can handle large RF signal. The flip side characteristics of PIN diode based switches are complex bias requirement, finite reverse recovery time, and non-compatibility of monolithic integration.

The inherent advantages of FET based switches over PIN Diode Switches are simplified bias network, small or negligible DC power requirement, simplified driver circuit, faster switching speed, monolithic implementation, ease of integrality with other functionality without the need of additional external components [54]. However, the power performance of a GaAs FET is limited by its current-handling capability in its low-impedance state and by its breakdown voltage in its high-impedance state [10]. And, for high reliability applications, maximum channel temperature should be restricted to <110°C to maintain higher MTBFs. Typical breakdown voltages for GaAs technology are around 6V (Low Noise process) to around 18V (Power process) and

maximum current carrying capacity of 0.4 A/mm to 0.7 A/mm, which are significantly on the lower side compared to PIN diode or GaN technology. GaN HEMT based devices, when compared to GaAs HEMT, have higher power handling capability, high breakdown voltage, and high thermal conductivity (GaN HEMT can be grown on SiC substrates), greatly helps the devices for high power density operation and are suitable for realization of high power switches [23]-[35].

To design high performance, high power GaAs FET T/R switches and absorptive receive protection switches which can handle few tens of Watts, using low power FET devices, various different circuit techniques are required to be employed. The power handling in the high impedance state, i.e., "OFF" FET case, is determined by gate-drain breakdown voltage, $V_{DG\ max,}$ and pinch-off voltage, $V_{p.}$ At larger input power levels, the RF voltage coupled to the gate will un-pinch the FET channel [10], causing it to start conducting and enters the non-linear region of operation. While the power handling capability of a FET switch in low impedance state is determined by peak drain-source saturation current, I_{DSS} [9][10]. Similar to the OFF FET case, for the ON FET case also, at larger input power levels, the RF voltage coupled to the gate will start pinching the FET channel and enters the non-linear region of operation. In this case, the positive gate bias, V_{GS}, shall be so chosen that, during the negative cycle excursion of input, the gate voltage shall not bring FET out of saturation, while during the positive cycle excursion, gate current shall not exceed the maximum limit. The other factor setting the limit for maximum power handling is the channel temperature rise, for the case of ON FET, due to thermal dissipation

2.1 Reported Techniques for increasing the Power Handling of a GaAs FET switch

Multiple techniques have been reported to increase the power handling capability of GaAs based switches/ limiters viz., reducing the voltage stress on the device using impedance transformation technique by placing the device (diode/FET) at a lower impedance point [9], [17], stacking number of FETs in series [10],[11],[13],[21], employing dual-gate FETs to mimic FET stacking [11], LC Resonators controlled by "ON" FETs to reduce the voltage stress on the device [14], employing wider FETs to increase the maximum current [11],[17] and distributed architecture employing stacked Schottky diodes [19],[20],[22]. The methods are briefly described below:

2.1.1 Impedance transformation technique

Ayasli et.al, [9] have reported a monolithic transmit-receive GaAs FET switch, with asymmetric switch configuration wherein both the Transmit and Receive arms can be determined independently, capable of switching more than 10 W CW power with about 1 dB insertion loss and 26 dB isolation at X-band frequencies, employing (a) wider FETs for increasing the I_{DSS}, (b) impedance transformation to keep the FETs at lower impedance to reduce the RF voltage swings in the Transmit path and (c) to keep the FETs at higher impedance to reduce the RF current in the Receive path for the given input power. Quarter wave transformers are used for the impedance transformation.

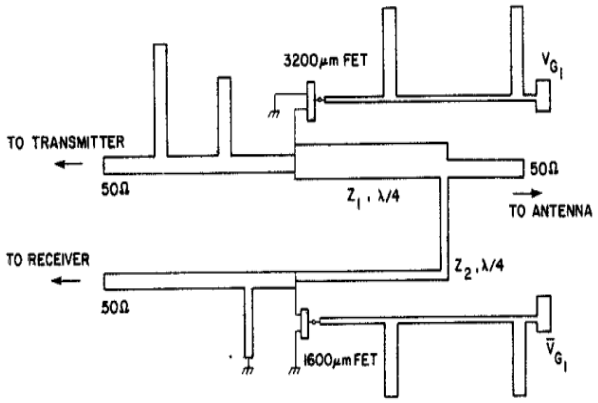

Figure 2-1. Schematic diagram of 10W T/R switch based on impedance transformation technique [9]

2.1.2 FET stacking technique

Mitchell B Schifrin et. al., [10] have reported "FET stacking", i.e., connecting the FETs in series to effectively distribute the total applied RF swing equally across all the series connected FETs. If the RF voltage swing is evenly divided within the stack FETs, the power handling capability increases as the square of the number of series stacked FETs. Fig. 2.2 shows the Stacked FET configuration proposed by Schiffrin et al.

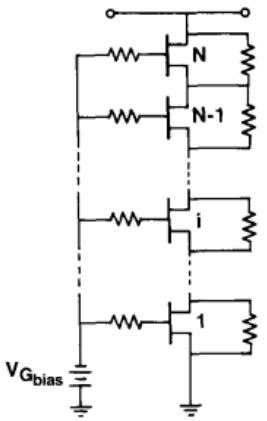

Figure 2-2. Schematic diagram of stacked FET circuit [10]

Employing this FET stacking technique along with inductive gate biasing, Katzin et al. [13] have demonstrated 100+ W RF switches. Mimicing of FET stacking using dual gate FETs has been proposed by M. J. Schindler et.al. [11]. Simplistically, a dual gate FET can be considered as two FETs connected in series, though significant coupling exists between the FETs.

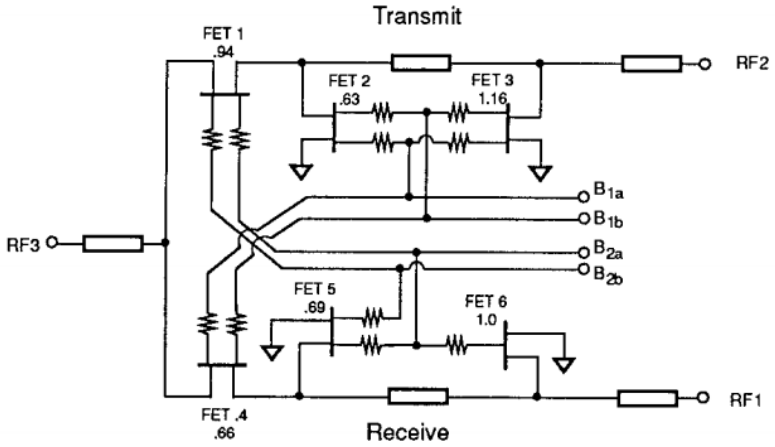

Figure 2-3. Schematic diagram of 2-18 GHz T/R switch using Dual Gate FETs [11]

2.1.3 Resonant Circuit Technique

As the typical breakdown voltage of GaAs FETs is significantly lower, the circuit can be made to employ switches only in ON state, as the power handling capability in ON state is limited by the peak drain-source saturation current (I_{DSS}). I_{DSS} can be increased by increasing the gate periphery viz. by employing wider FETs.

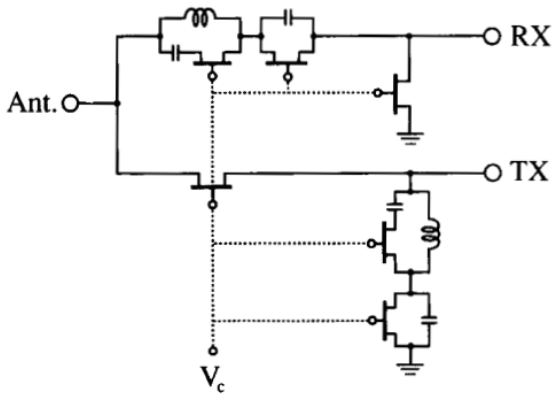

Figure 2-4. T/R switch employing FET switchable LC resonators [14]

T.Tokimitsu et al., [14] employed an LC resonator technique to effectively create "parallel resonance" employing FET switched shunt inductors and series/shunt capacitors, as shown in Fig. 2-4, thus operating the FETs only in ON state. This

technique overcomes the low break down voltage limit of FETs, for realizing high power switches.

2.1.4 Distributed FET/Diode technique

This technique has been commonly used for the implementation of high power switches, limiters etc., where the FETs / Schottky diodes are distributed uniformly along the transmission line. The device sizing is done non-uniformly along the transmission line, to ensure that all the diodes / FETs operate at the respective maximum allowed current conditions, under application of high power. D. P. Nguyen et al., [21], have employed distributed, stacked FET configuration, as shown in Fig. 2-5, for demonstrating a 4W T/R Switch at K-band.

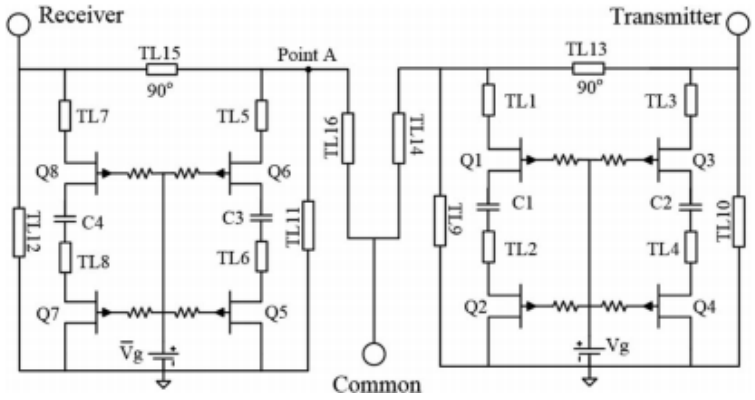

Figure 2-5. Schematic of T/R switch employing distributed, stacked FETs [21]

P. Mahmoudidaryan et al., [22], have employed distributed FET technique, as shown in Fig. 2-6, and have exploited the gate-drain coupling to realize a 5W limiter.

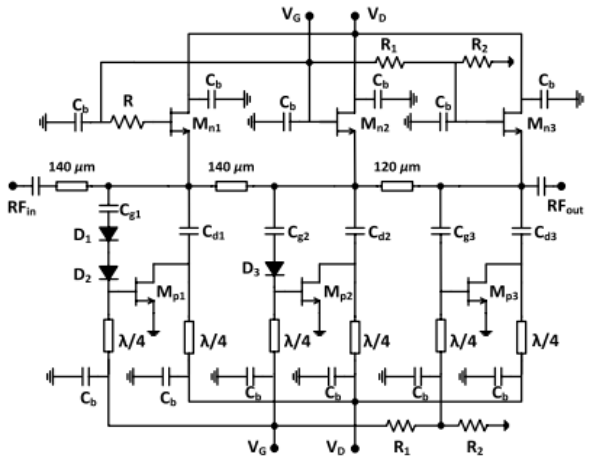

Figure 2-6. Schematic of Distributed, FET limiter [19]

2.1.5 Balanced configuration technique

I.J. Bahl [17] has employed a balanced configuration coupled with impedance transformation using Schottky diodes to realize a 10W Limiter/LNA, whose schematic shown in Fig. 2-7. In this configuration, limiters in each of the arms of hybrid need to handle only half the input power. Impedance transformation is done to keep the diodes at low impedance point to reduce the voltage stress on the device.

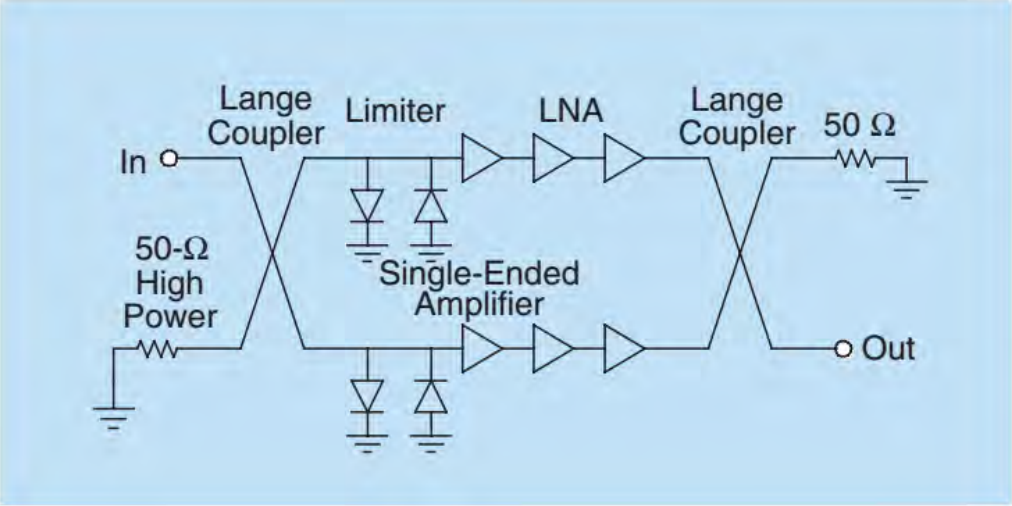

Figure 2-7. Schematic of Balanced Limiter/LNA [17]

2.1.6 Distributed, Terminated technique

A.P.M. Maas et al.,[19], have employed the above technique, with distributed terminated GaAs Schottky diodes of PPH25X power process of UMS, for demonstrating limiting up to 4W. Fig. 2-8 shows the schematic of distributed, terminated diode limiter.

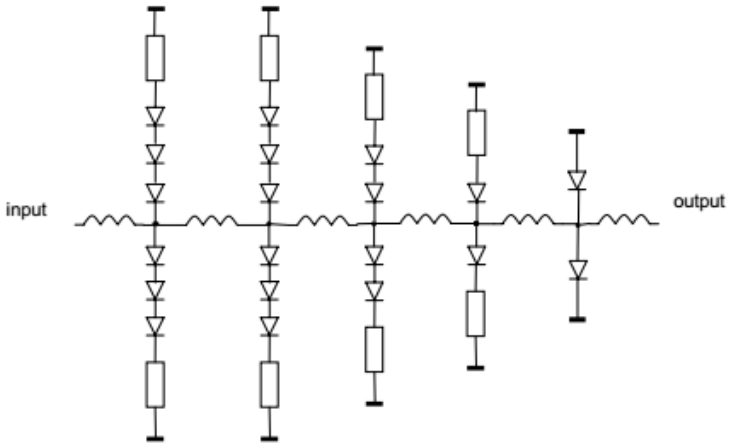

Figure 2-8. Schematic of Distributed, terminated schottky diode limiter [19]

Mitchell B Schifrin et al., [10] have reported a “Distributed, terminated FET

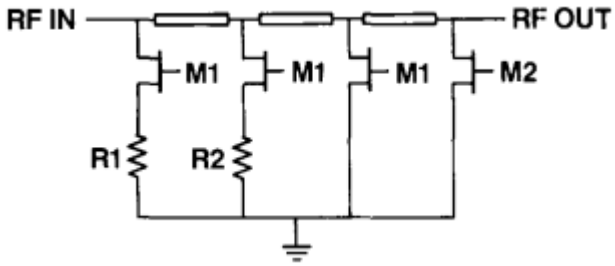

Figure 2-9. Schematic of Distributed, terminated FET SPST switch [10]

based SPST” switch, whose schematic is shown in Fig. 2-9.

In this configuration, the shunt switches, terminated with high power termination, are ON during the high power transmission, thus absorbing the power during protection mode. The distributed structure is employed to increasing power handling capability and to increase the isolation.

2.1.7 GaN HEMT based switches

Due to high field breakdown capability, GaN based switches are capable of high voltage operation. The switch technology is particularly being used for high power applications. The CW power handling capabilities are comparable with PIN diodes while having low power dissipation like GaAs and Si transistors [54]. Various high power switches using GaN technology have been reported [23] - [35].

All the above circuit based techniques, described above, can be employed for increasing the power handling capability of GaN based Switches, beyond the individual GaN FET capabilities.

Hangai,M et al. [23] have employed asymmetric switch configuration, along with impedance transformation proposed by Ayasli et.al [9], whose schematic is given in Fig. 2-10, for demonstrating 100W protection switch.

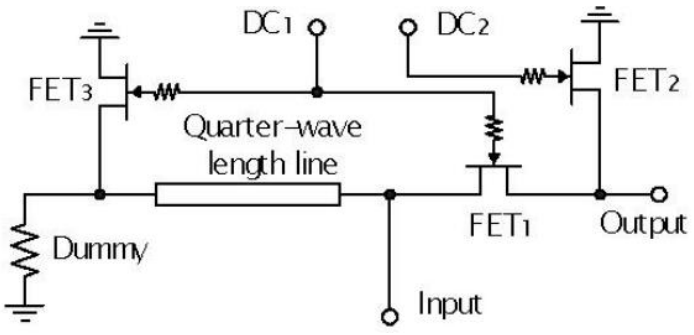

Figure 2-10. Schematic of asymmetric GaN T/R switch [23]

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Chapter: 3

Design Approach and Analysis

3.0 Introduction

The aim of the present research is to devise techniques for high power T/R switches employing low power and low noise GaAs pHEMT processes. And also to employ these techniques to design higher power T/R switches using GaN pHEMT process.

Subsequent sections cover the basic power handling capability of a FET switch, method to increase the power handling capability, and various novel techniques to improve the RF performance of the switch.

3.1 Power Handling of a FET switch:

The equivalent circuit of a resonant shunt FET switch is given in Fig. 3-1, where R_{DS} is the drain source resistance, C_{DS}, C_{DG} and C_{GS} are the drain-source, drain-gate and gate-source capacitances respectively. R_{DS}, C_{DG} and C_{GS} are gate bias dependent elements with $C_{DG} \cong C_{GS}$, while C_{DS} is a significant parasitic capacitance affecting the insertion loss and isolation performance of the switch. C_{DS} is parallel resonated with a shunt inductor, L_{DS}, connected across drain and source terminals, making it a resonant switch at the operating frequency. R_G is an external gate bias resistance.

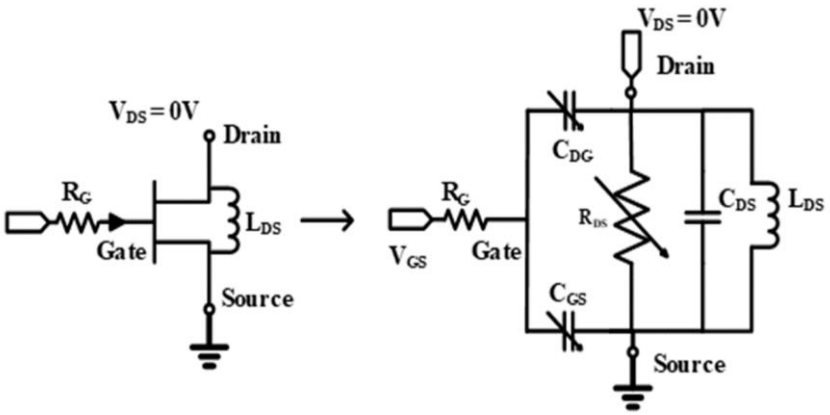


Figure 3-1. Equivalent circuit of resonant shunt FET switch

When, gate-source voltage, $V_{GS} \leq$ pinch-off voltage, V_p, FET is OFF and presents high value shunt resistance, $R_{DS\ OFF}$, while with $V_{GS} \geq 0$, FET is ON and acts like short with a small shunt resistance, $R_{DS\ ON}$.

The power handling in the high impedance state, i.e., "OFF" FET case is determined by gate-drain breakdown voltage, $V_{DG\ max}$, and V_p. An instantaneous input voltage across the off-state shunt switch is voltage divided by the gate-source (C_{GS}) and gate-drain capacitances (C_{DG}). For symmetrical location of gate in the transistor, $C_{DG} \cong C_{GS}$, the coupled gate voltage is half of RF input applied across the drain terminal of the device. At larger input power levels, the RF voltage coupled to the gate will un-pinch the FET channel causing it to start conducting and enters the non-linear region of operation, as shown in Fig. 3-2.

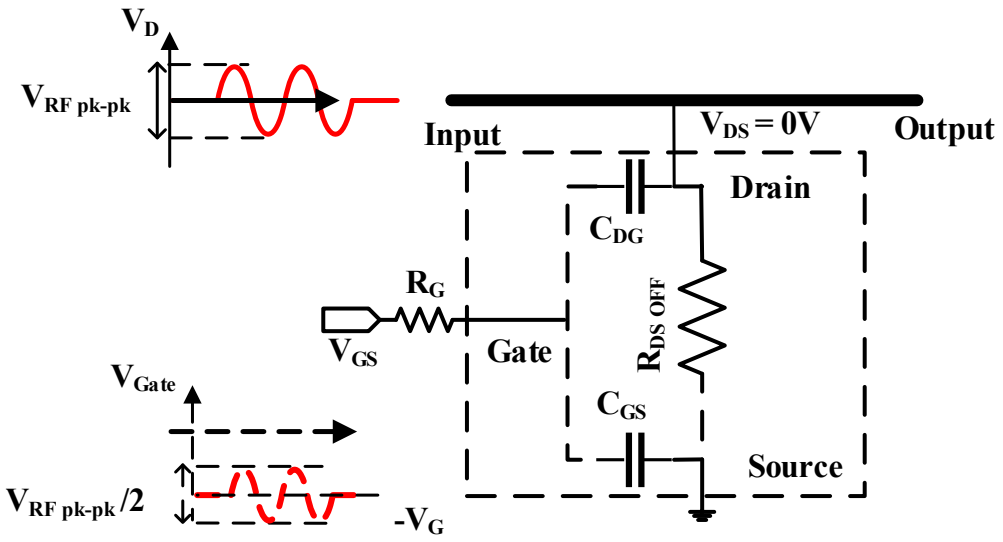


Figure 3-2. Gate – Drain coupling equivalent circuit of OFF shunt FET

The control voltage, $|V_{GS}|$, at the shunt FET gate, needs to be set large enough to keep the FET pinched-off even with the superimposed RF signal coupled on the gate. Optimal negative gate bias, V_{GS}, shall be so chosen that, during the positive cycle excursion of input, the gate voltage shall not bring FET out of pinch-off, while during the negative cycle excursion, gate-drain voltage, V_{DG}, shall not exceed the $V_{DG\ max}$. So as the RF voltage on the gate is allowed to swing from $V_{DG\ max}$ to V_p, which is half of the applied RF input, the optimal V_{GS} lies in the middle of this range. This yields the approximation [2] of the shunt FET power handing capability in OFF state as given in (3.1), for the optimal gate bias voltage:

$$\text{Matched Load Pmax\_OFF\_state} = \frac{(V_{DG\ max} - |V_P|)^2}{2Z_0} \tag{3.1}$$

where Z_0=system impedance, V_p=pinch-off voltage. However, depending on the load impedance, Z_L, the above equation gets modified reducing maximum power handling for $Z_L > Z_0$, and is given by:

$$\text{Pmax\_OFF\_state} = \frac{(V_{DG\,max} - |V_P|)^2}{2Z_0} * \left(\frac{1+\frac{Z_0}{Z_L}}{2}\right)^2 \quad (3.2)$$

The power handling capability of a FET switch in low impedance state is determined by peak drain-source saturation current, I_{DSS} [8]. Because of non-zero and finite ON resistance, $R_{DS\,ON}$, of FET, the current passing through shunt ON FET will be less than the short circuit current. And so, the power handling capability in ON state for a shunt FET, for a given $R_{DS\,ON}$, is given by:

$$\text{Pmax}_{\text{ON}_{\text{state}}} = \frac{Z_0 (I_{DSS})^2}{2} * \left(\frac{1+\frac{R_{DS\,ON}}{Z_L}}{2}\right)^2 \quad (3.3)$$

In low impedance state also, the non-linearity sets in with increasing input RF power because of coupled gate voltage. The instantaneous voltage developed across drain-source terminals is coupled to the gate through potential division by the C_{GS} and C_{DS}, as shown in Fig. 3-3.

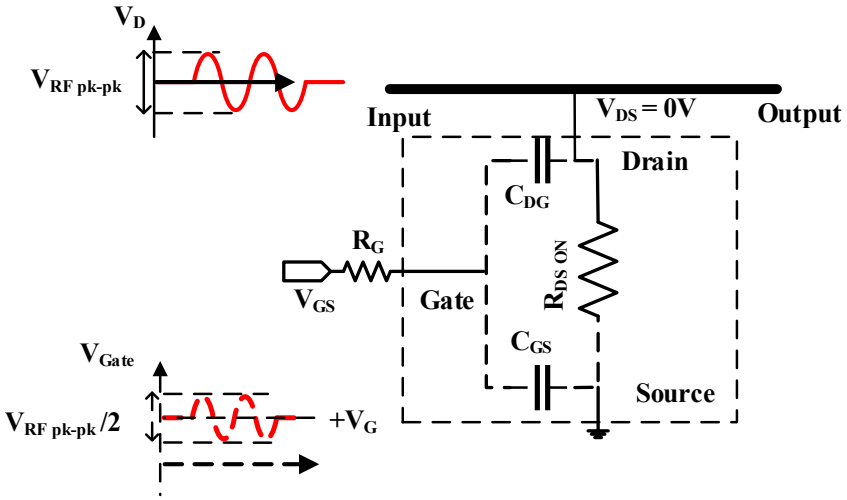


Figure 3-3. Gate – Drain coupling equivalent circuit of ON shunt FET.

In this case, the positive gate bias, V_{GS}, shall be so chosen that, during the negative cycle excursion of input, the gate voltage shall not bring FET out of saturation, while during the positive cycle excursion, gate current shall not exceed the maximum limit. This yields the following approximation of the peak $I_{DS\,max}$ allowed before coupled RF gate voltage starts modulating the $R_{DS\,ON}$, in low impedance state, for linear range of operation of switch,

$$I_{DS\,max.\,pk} = \frac{2V_{GS}}{R_{DS\,ON}} \quad (3.4)$$

The other factor setting the limit for maximum power handling is the channel temperature rise, for the case of ON FET, due to thermal dissipation and is given by:

$$T_{j\,rise} = \frac{I_{DS\,pk-pk}{}^{2} * R_{DS\,ON} * \theta_j}{8} \quad (3.5)$$

where, θ_j is the channel thermal resistance in °C/W.

3.2 Increasing the Power Handling of a FET switch

Multiple techniques have been reported to increase the power handling capability of GaAs based switches/ limiters viz., reducing the voltage stress on the device using impedance transformation technique by placing the switching field effect transistor (FET) at a lower impedance point, stacking number of FETs in series, employing dual-gate FETs to mimic FET stacking, LC Resonators controlled by "ON" FETs to reduce the voltage stress on the device, employing wider FETs to increase the maximum current, distributed architecture employing stacked Schottky diodes. In the present work, extending and modifying the work of Schiffrin et.al., [8] on the terminated SPST high power switch, on-the-chip coherent current distribution technique is employed to increase the power handling capability in low impedance state.

3.2.1 On-the-Chip Coherent Current Distribution Technique

Observing the linear region maximum power handling condition and also the junction temperature rise, given in equations (3.4) and (3.5), if the current through each device, I_{DS}, for a given input power, can be reduced by distributing current across multiple devices, i.e., coherent current paralleling, then the switch can be made to handle large power in low impedance state as shown in Fig. 3-4.

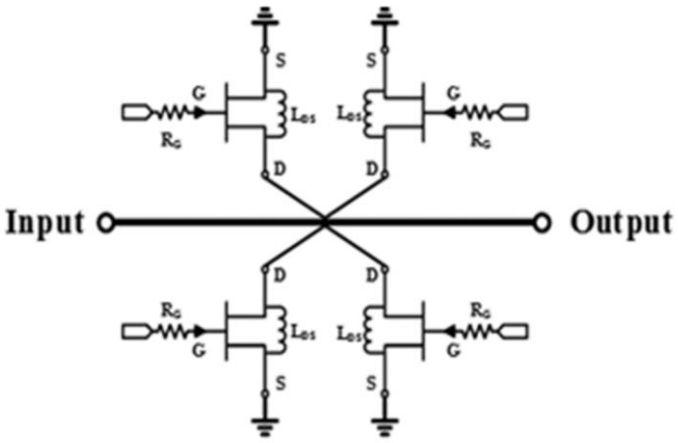


Figure 3-4. On-the-Chip Coherent Current Distribution

In the proposed approach, the current is divided, coherently, across identically sized N number of W gate width devices connected to a common node in a star configuration. The equivalent circuit of star connected identical N number of paralleled W gate width devices is same as that of a single FET with gate periphery of N*W;

however, the paralleled approach has the significant advantage of distributed power dissipation across multiple devices as compared to entire dissipation in a single large device. The other advantage is that it is a scalable architecture and so can be employed for handling very large powers, employing low power devices.

3.2.1.1 Selection of number of devices for paralleling

Though paralleling of devices increases the power handling capability by N^2 times that of an individual device, but due to paralleling the effective R_{DSON} and R_{DSOFF} are the parallel combination of N devices of unit cell R_{DSON} and R_{DSOFF}. Lower R_{DSON} improves both transmit path insertion loss and receive isolation in high power mode, but as R_{DSOFF} is also reduced the receive path loss increases. Hence, the no. of devices to be paralleled is a trade-off between the allowable transmit and receive path losses and the power handling capability. Also, *due to the physical size of transistor, and also the need to have all the gates aligned in same direction for fabrication of the devices, it is not possible to connect more than two FETs directly to a common node*. So, for increasing the number of devices to be paralleled, two number of node connected FETs are used as unit cell and such cells are connected to a common node through a shortest possible equal length transmission line, TL_I, in a star configuration. The inductance of this unavoidable interconnect line transforms the impedances offered by FET, thus degrading receive path loss in high impedance state and the transmit loss and isolation in low impedance state. To compensate the inductance of TL_I, a capacitance C_T is added to series resonate the parasitic inductance of this finite length TL_I [2]. The schematic and equivalent circuit of interconnect compensated, current paralleled FET is shown in Fig. 3-5 (a) and (b) respectively, where TL_I is the interconnect line.

When N no. of identical devices are paralleled, the effective drain-source resistances are $R_{DS\ ON\ eff} = R_{DS\ ON}/N$ and $R_{DS\ OFF\ eff} = R_{DS\ OFF}/N$ and the maximum current is $N*I_{DSS}$. Hence the power handling for current distributed configuration is

$$P_{max-ON-distributed} = \frac{Z_o(N*I_{DSS})^2}{2}\left(\frac{(1+\frac{R_{DS\ ON}}{N*Z_0})}{2}\right)^2 \quad (3.6)$$

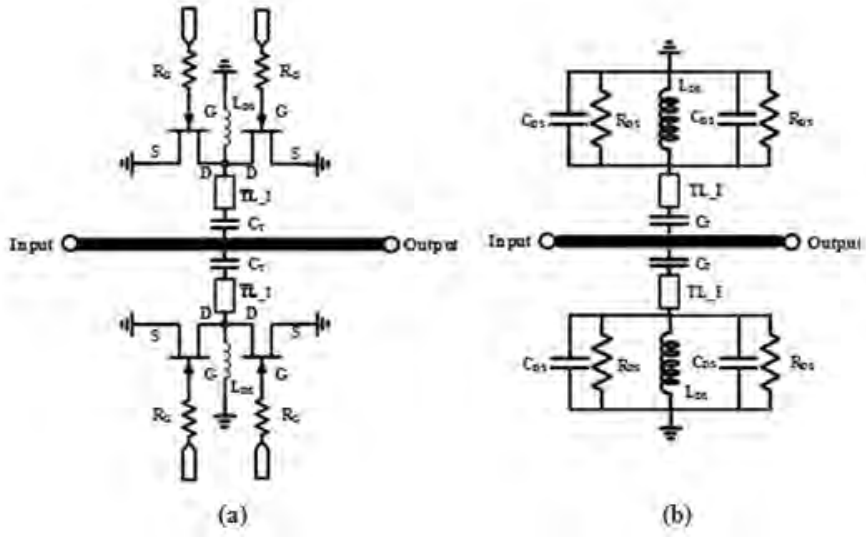


Figure 3-5. Interconnect compensated, 4 shunt FET current paralleled SPST element (a) Schematic (b) Equivalent circuit

3.2.2 T/R switch / Receive Protection Switch Architecture

Employing the high power shunt switch element, described in the earlier section, a double pole double throw (DPDT) switch, with at least one of the paths capable of handling high power, can be used as a T/R switch or an absorptive receive protection switch. In the present work, a DPDT structure is realized with shunt switches in a balanced configuration where two identical single pole single throw (SPST) switch elements form each arm enclosed by quadrature hybrids at input and output, as shown in the Fig. 3-6.

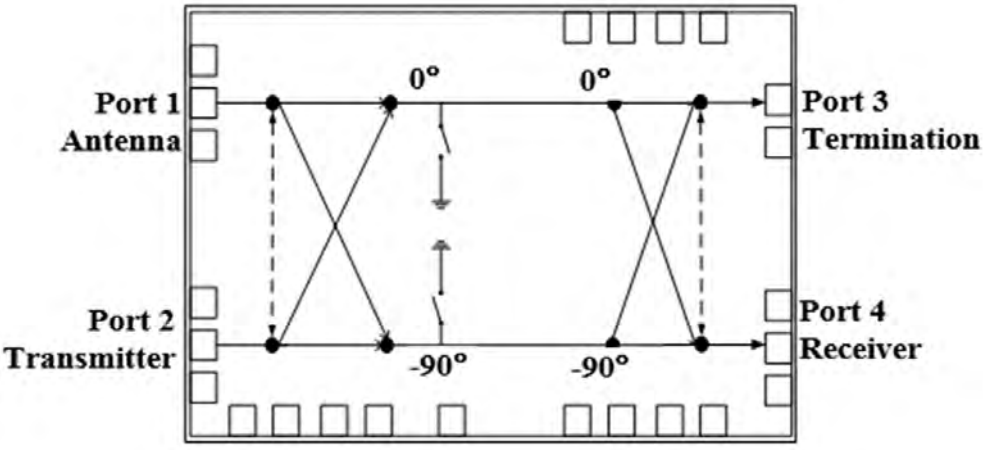


Figure 3-6. Block schematic of TR Switch / Receive protection switch

Because of the balanced structure, each of the switch elements handles only half the input power and also overall structure has good input and output return losses. In

Transmit mode, the switches are ON, offering short circuit and full power fed from Port 2 (Transmitter) gets reflected from both the identical switches and routed to Port 1 (Antenna), isolating the Port 4 (receiver). The total transmit loss is the sum of twice the input hybrid loss and the return loss of the shunt switch in ON state. While, during receive mode, switches are open, offering high shunt resistance and signal fed from Port 1 (Antenna) passes through to Port 4 (receiver). The total receive loss is the sum of insertion losses of input hybrid, output hybrid and insertion loss of the shunt switch in OFF state. For the case of application as an absorptive receive protection switch, a ferrite circulator is employed for time division duplexing of PA and LNA, as shown in Fig. 1-2, and hence, Port 1 is connected to Antenna via circulator while Port 2 is terminated in an off chip high power termination, thus isolating and protecting the receiver during transmit mode, from antenna reflected power.

The drawback of the S-matrix is that it is limited to not having a direct cascading relationship. Hence, the shunt FET enabled DPDT, as shown in Fig. 3-6, can be analyzed by employing T-parameters technique [1]. The effect of cascading multiport network is found by simply multiplying sequentially associated T-matrices. T-parameter relates voltage waves at input port to voltage waves at output port. Equation (3.7) shows the definition of T-parameter for an $m\ X\ n$ port network.

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_m \\ a_1 \\ a_2 \\ \vdots \\ a_m \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} & \cdots & T_{1N} \\ T_{21} & T_{22} & \cdots & T_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ T_{M1} & T_{M2} & \cdots & T_{MN} \end{bmatrix} \begin{bmatrix} a_{(m+1)} \\ a_{(m+2)} \\ \vdots \\ a_{(m+n)} \\ b_{(m+1)} \\ b_{(m+2)} \\ \vdots \\ b_{(m+n)} \end{bmatrix} \tag{3.7}$$

where b_k, a_k are the reflected and incident voltage wave at Port K and T_{mn} is the T-parameter between the input port, m and the output port, n. T-matrix of cascaded p numbers of n port network is given by:

$$T_M = T_1\, T_2\, \ldots\ldots T_p$$

where T_i is the T-parameter of the i^{th} network. From (3-7), two port T-parameter and its comparison with two port S-parameter is given by:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.8}$$

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{21} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \tag{3.9}$$

By applying linear algebra, conversion formula of 2-port S-parameter to T-Parameter and vice-versa is given by:

$$\begin{bmatrix} S_{11} & S_{21} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} T_{12}.{T_{22}}^{-1} & T_{11} - T_{12}.{T_{22}}^{-1}T_{21} \\ {T_{22}}^{-1} & -{T_{22}}^{-1}T_{21} \end{bmatrix} \tag{3.10}$$

$$\begin{bmatrix} T_{11} & T_{21} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} S_{12}.-S_{11}.{S_{21}}^{-1}S_{22} & S_{11}.{S_{21}}^{-1} \\ -{S_{21}}^{-1}.S_{22} & {S_{21}}^{-1} \end{bmatrix} \tag{3.11}$$

T-parameter of balanced 4-port network, due to symmetry, is divided into 4 quadrants $[T(I,I)\,], [T(I,II)\,], [T(II,I)\,], [T(II,II)\,]$, where each quadrant is equivalent to $T_{11}, T_{12}, T_{21}, T_{22}$ of 2-port T-parameter.

$$\begin{bmatrix} \overbrace{\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix}}^{T_{[I,I]}} & \overbrace{\begin{bmatrix} T_{13} & T_{14} \\ T_{23} & T_{24} \end{bmatrix}}^{T_{[I,II]}} \\ \underbrace{\begin{bmatrix} T_{31} & T_{32} \\ T_{41} & T_{42} \end{bmatrix}}_{T_{[II,I]}} & \underbrace{\begin{bmatrix} T_{33} & T_{34} \\ T_{43} & T_{33} \end{bmatrix}}_{T_{[II,II]}} \end{bmatrix} \Rightarrow \begin{bmatrix} [T_{I,I}] & [T_{I,II}] \\ [T_{II,I}] & [T_{II,II}] \end{bmatrix} \tag{3.12}$$

S to T-parameter conversion for 4-port symmetrical network is obtained by substituting (3-8) and (3-10) in (3-11) and is given by:

$$\begin{bmatrix} [S_{I,I}] & [S_{I,II}] \\ [S_{II,I}] & [S_{II,II}] \end{bmatrix} = \begin{bmatrix} [T_{I,II}].[T_{II,II}]^{-1} & [T_{I,I}] - [T_{I,II}].[T_{II,II}]^{-1}[T_{II,I}] \\ [T_{II,II}]^{-1} & -[T_{II,II}]^{-1}[T_{II,I}] \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} [\mathrm{T}_{11}] & [\mathrm{T}_{21}] \\ [\mathrm{T}_{21}] & [\mathrm{T}_{22}] \end{bmatrix} = \begin{bmatrix} [\mathrm{S}_{\mathrm{I,II}}] - [\mathrm{S}_{\mathrm{I,I}}].[\mathrm{S}_{\mathrm{II,I}}]^{-1}[\mathrm{S}_{\mathrm{II,II}}] & [\mathrm{S}_{\mathrm{I,I}}].[\mathrm{S}_{\mathrm{II,I}}]^{-1} \\ -[\mathrm{S}_{\mathrm{II,I}}]^{-1}.[\mathrm{S}_{\mathrm{II,II}}] & [\mathrm{S}_{\mathrm{II,I}}]^{-1} \end{bmatrix} \tag{3.14}$$

where $[S(I,I)\,], [S(I,II)\,], [S(II,I)\,], [S(II,II)\,]$ are four quadrants of four port S-parameter.

Applying the equivalent circuit of resonant shunt FET, given in Fig. 3-1, the proposed T/R switch block diagram is shown in Fig. 3-7.

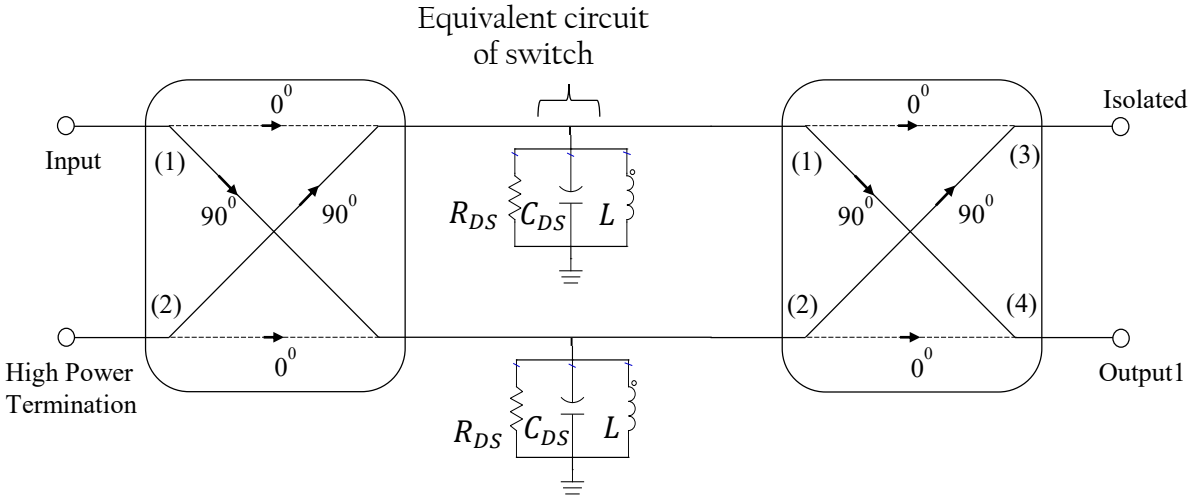


Figure 3-7. Schematic of proposed resonant shunt FET enabled high-power T/R switch

where R_{DS}, C_{DS}, L are shunt FET channel resistance, drain to source capacitance and shunt inductor to resonate C_{DS}. The impedance, Z of shunt FET with a shunt inductor is given by:

$$Z = \frac{jR_{DS}X}{R_{DS}+jX} \tag{3.15}$$

where $X = j\frac{\omega L}{1-\omega^2 LC_{DS}}$ is the effective shunt reactance due to channel capacitance and shunt inductor.

S-parameter of input and output quadrature hybrid and four port shunt switch is given by:

$$[S]_{Hybrid} = \frac{1}{\sqrt{2}}\begin{bmatrix} 0 & 0 & 1 & -j \\ 0 & 0 & -j & 1 \\ 1 & -j & 0 & 0 \\ -j & 1 & 0 & 0 \end{bmatrix} \tag{3.16}$$

$$[S]_{SwitchNetwork} = \begin{bmatrix} \frac{-Z0}{Z0+2Z} & 0 & \frac{2Z}{Z0+2Z} & 0 \\ 0 & \frac{-Z0}{Z0+2Z} & 0 & \frac{2Z}{Z0+2Z} \\ \frac{2Z}{Z0+2Z} & 0 & \frac{-Z0}{Z0+2Z} & 0 \\ 0 & \frac{2Z}{Z0+2Z} & 0 & \frac{-Z0}{Z0+2Z} \end{bmatrix} \tag{3.17}$$

where Z_0 is the characteristic impedance of the system.

To evaluate the cascaded network S-parameter, each of the above four port network S-parameter is converted into T-parameter and cascaded T-parameter provides the four port S-parameter of the entire network. Cascaded T-parameter, $T_{Cascaded}$, of Fig. 3-7 is given by:

$$T_{Cascaded} = \begin{bmatrix} 0 & -j\left(\frac{2Z}{Z0+2Z} - \frac{Z0^2}{(Z0+2Z)2Z}\right) & \frac{-Z0}{2Z} & 0 \\ -j\left(\frac{2Z}{Z0+2Z} - \frac{Z0^2}{(Z0+2Z)2Z}\right) & 0 & 0 & \frac{-Z0}{2Z} \\ \frac{Z0}{2Z} & 0 & 0 & j\left(\frac{Z0+2Z}{2Z}\right) \\ 0 & \frac{Z0}{2Z} & j\left(\frac{Z0+2Z}{2Z}\right) & 0 \end{bmatrix} \quad (3.18)$$

Using (3.18) and (3.13), S-parameter, $S_{cascaded}$, of proposed high power protection switch is given by:

$$[S_{cascaded}] = \begin{bmatrix} 0 & j\frac{Z0}{Z0+2Z} & 0 & -j\frac{2Z}{Z0+2Z} \\ j\frac{Z0}{Z0+2Z} & 0 & -j\frac{2Z}{Z0+2Z} & 0 \\ 0 & -j\frac{2Z}{Z0+2Z} & 0 & j\frac{-Z0}{Z0+2Z} \\ -j\frac{2Z}{Z0+2Z} & 0 & j\frac{-Z0}{Z0+2Z} & 0 \end{bmatrix} \quad (3.19)$$

From (3.19), the insertion loss and isolation port transmission coefficient of the protection switch is given by

$$\text{Receive Path Loss } = |S_{41}| = \left|\frac{2Z}{Z_0 + 2Z}\right| \quad (3.20)$$

$$\text{Transmit Path Loss } = |S_{21}| = \left|\frac{Z_0}{Z_0 + 2Z}\right| \quad (3.21)$$

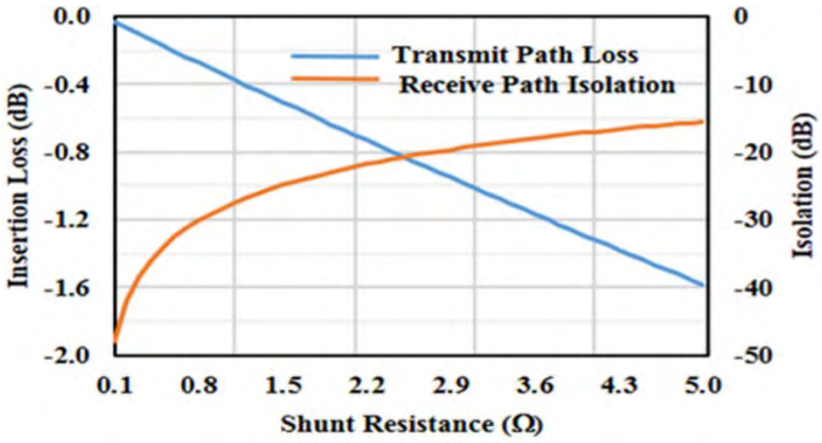
From (3.20) and (3.21) it is evident that when the shunt FET is 'OFF', ideally $Z = \infty$, all power is transmitted to Port4 and insertion loss is minimum whereas when the FET is ON, ideally $Z = 0$ and all the power is reflected to Port 2 which is terminated using a high power load resistor.

The phase response of switch in insertion loss state and isolation state is given by:

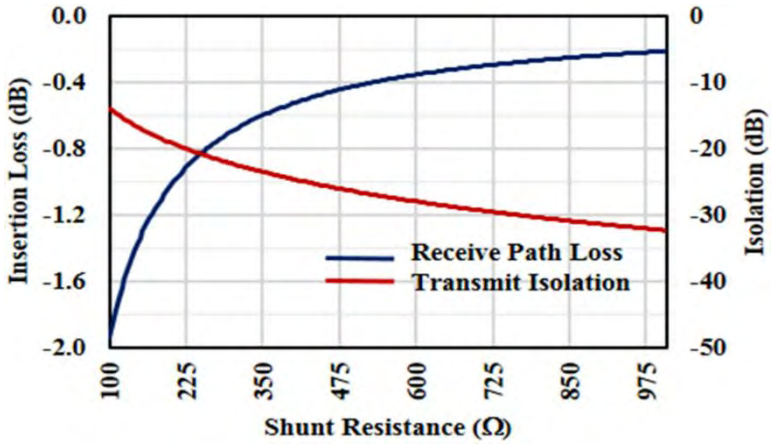
$$\angle\text{Receive Path } = \angle S_{41} = \tan^{-1}\left(\frac{Z_0X + 2RX}{Z_0R}\right) \quad (3.22)$$

$$\angle\text{Transmit Path } = \angle S_{41} = 90^0 - \tan^{-1}\left(\frac{Z_0X + 2RX}{Z_0R}\right) + \tan^{-1}\frac{X}{R} \quad (3.23)$$

When shunt inductor resonates with drain to source channel capacitance, $X = \infty$ $\angle S_{41} = -90^0$ and $\angle S_{21} = 90^0$. Utilizing (3.20) and (3.21), Fig. 3-8(a) and (b) shows the analyzed transmit and receive mode performance of T/R Switch as a function shunt resistance R, with ideal input and output hybrids.



(a)



(b)

Figure 3-8. Performance of T/R switch as a function shunt resistance. (a) Transmit Mode (b) receive mode

Hence, during high power transmit, the switch is closed with $R=R_{DS\ ON,}$ which is of the order of few ohms, routing the power from Port 2 (Transmitter) to Port 1 (Antenna) with low loss, while isolating the Port 4 (Receiver). During receive, the switch is opened, $R=R_{DS\ OFF,}$ which is of the order of few hundreds of ohms, routing the power from Port 1 (Antenna) to Port 4 (Receiver), thus creating low loss Transmit/Receive Switch.

Applying the analysis carried out, the following cases are examined to estimate the power handling capability and RF performance of T/R Switches.

3.2.2.1 Case -1: 10W T/R Switch using 0.25µm GaAs pHEMT (PH25-M/s UMS)

For monolithic integration of an LNA and high power T/R switch, the device process shall be so chosen to have the lowest F_{min}, minimum Noise Figure at optimal source reflection coefficient, Γ_{opt}, at the operating frequency, which is inherently a low power process. One of the chosen standard low noise pHEMT process (PH25), is having typical parameters like V_p =-0.75V, V_{DS} max=7V, I_{DSS} typ.=350mA/mm, largest

characterized gate periphery of 600 µm (8x75µm), Θj =150°C/W with $R_{DS\ ON}$= 4.0Ω and $R_{DS\ OFF}$ = 560Ω. For most of GaAs processes, the I_{DSS} variation across a wafer and across batches is as high as 30% and hence the design has to be made for $I_{DSS\ typical}$ rather than $I_{DSS\ max}$. For the chosen process, the $I_{DSS\ max}$ = 500 mA/mm and hence, conservative $I_{DSS\ typical}$ of 350mA/mm is used for design. This process, in conventional configuration, yields a unit cell switch which has a Pmax of 0.3W in low impedance state. The maximum power handling capability of T/R switch with two different I_{DSS} values, transmit path and the receive path losses, receive isolation of complete T/R switch, as a function of no. of devices paralleled, calculated using equations (3.20) and (3.21) for the typical process chosen, with ideal input and output hybrids, is given in the following Fig. 3-9 and Fig. 3-10.

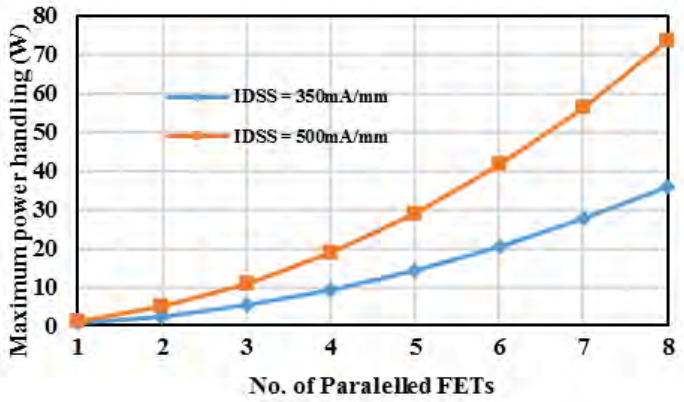


Figure 3-9. Maximum power handling capability of GaAs T/R Switch (PH25- UMS) with two different I_{DSS}, as a function of no. of devices paralleled.

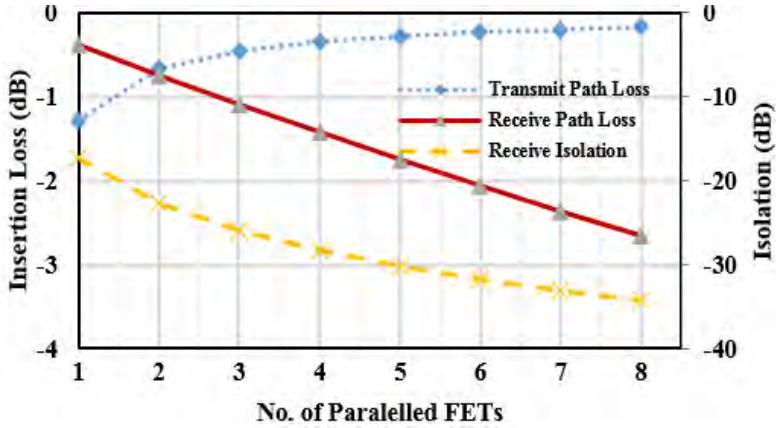


Figure 3-10. GaAs T/R Switch performance as a function of no. of devices

As can be seen from Fig. 3-9 and Fig. 3-10, a 300mW power handling capable FET device is employed to realize a 10W T/R Switch, with coherent current distribution across 4 identical devices, having transmit loss of 0.4 dB with receive isolation of 28 dB and receive loss of 1.4 dB.

3.2.2.2 Case -2: 200W T/R Switch using 0.25µm GaN pHEMT (GH25-M/s UMS)

As GaN process is also suitable for realizing LNAs, due to its lower noise figure, the on-the-chip coherent current distribution technique is employed for designing a 200W T/R Switch using 0.25µm GaN pHEMT process from UMS (GH25-10), which has parameters like Vp=-3.5V, V_{DSmax}=90V @ V_{GS}=-20V, $I_{DSS\ typ.}$=1000mA/mm. *When used in ON state, the linear power handling capability, for widest 800 µm single shunt FET, is 3.1W and the switch can be controlled using 0/-4V only.* The typical R_{DSON} and $R_{DS\ OFF}$ are 6.0 and 1000Ω respectively for this device. The maximum power handling capability, transmit path and the receive path losses, receive isolation of complete GaN T/R switch, as a function of number of devices paralleled, is calculated using equations (3.18) and (3.19) for the typical process chosen, with ideal input and output hybrids, and is given in the following Fig. 3-11 and Fig. 3-12.

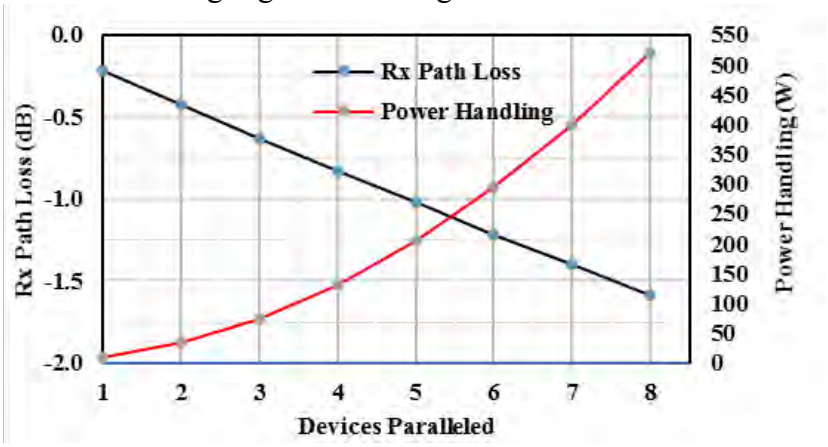


Figure 3-11. Maximum power handling capability of GaN T/R Switch (GH25- UMS) and Receive path loss as a function of no. of devices paralleled

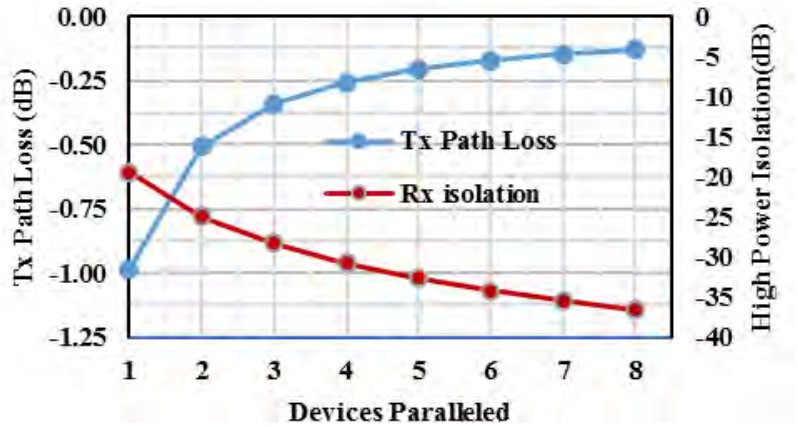


Figure 3-12. Transmit path loss and Receive isolation as a function of no. of devices paralleled, for GaN T/R Switch (GH25- UMS)

From Fig. 3-11, for handling 200W power, six devices need to be paralleled.

However, as discussed in section 3.2.1.1, 8 devices are necessary for coherent current distribution. *It can be seen from Fig. 3-11 and Fig. 3-12, a 3.1W power handling capable GaN FET device is employed to realize a 525 W T/R Switch with coherent current distribution across 8 identical devices having transmit loss of 0.15 dB with receive isolation of 35 dB and receive loss of 1.6 dB.* However, as the no. of devices paralleled is increased, the power handling capability is significantly enhanced, but the receive path loss also increases significantly due to reduced $R_{DS\ OFF\ eff.}$ *Hence a novel impedance transformation technique along with on-chip coherent current distribution is devised to improve the receive path loss without significantly affecting the power handling capability.*

3.2.3 High power T/R switch employing impedance transforming technique and on-the-chip coherent current distribution technique

Conventionally, the impedance transformation technique is employed to increase the power handling capability of "OFF" FET switches by placing the shunt FET at a lower impedance point. As the shunt FET operates at lower impedance point, the voltage swing generated across its drain to source channel reduces, resulting in high power handling capability of the switch. **However, in the proposed technique, the step-down impedance transformation is employed to improve the receive path loss, while power handling capability is achieved by on-the chip coherent current distribution, extending and modifying the work of Bahl [7] on the absorptive Limiter/LNA.** An impedance transforming quadrature hybrid at input and output is used to transform the impedance from Z_0 to lower impedance and lower impedance to Z_0 respectively. Fig. 3-13 shows the block schematic of high power T/R switch employing impedance transforming technique.

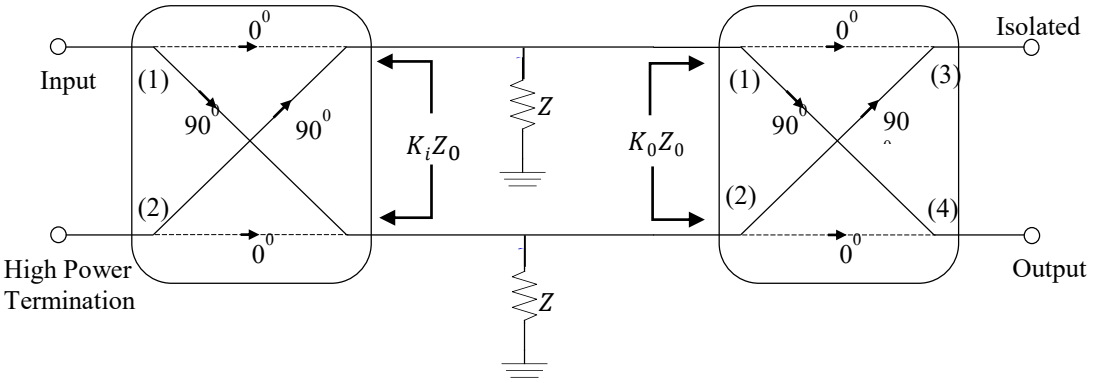


Figure 3-13. Block schematic of high-power switch employing impedance transforming technique

Shunt FET switch in each arm is represented by its equivalent impedance, Z where as K_i, K_0 are input and output quadrature hybrid impedance transformation ratios and is given by:

$$K_i = \frac{Z_{\,OP\ impednace\ of\ IP\ hybrid}}{Z_0} \tag{3.24}$$

$$K_0 = \frac{Z_{IP\ impedance\ of\ OP\ Hybrid}}{Z_0} \tag{3.25}$$

As carried out in the previous section, the circuit is analysed using T-parameter technique. To obtain the T-parameter of each of the cascaded networks, S-parameters of input hybrid, switch network and output hybrid are derived. Equation (3.26) and (3.27) shows the S-parameter of input and output quadrature hybrid respectively.

$$[S]_{IP\ Hybrid} = \begin{bmatrix} 0 & 0 & -j & -1 \\ 0 & 0 & -1 & -j \\ -j & -1 & \frac{K_i - 1}{K_i + 1} & 0 \\ -1 & -j & 0 & \frac{K_i - 1}{K_i + 1} \end{bmatrix} \tag{3.26}$$

$$[S]_{OP\ Hybrid} = \begin{bmatrix} \frac{K_0 - 1}{K_0 + 1} & 0 & -j & -1 \\ 0 & \frac{K_0 - 1}{K_0 + 1} & -1 & -j \\ -j & -1 & 0 & 0 \\ -1 & -j & 0 & 0 \end{bmatrix} \tag{3.27}$$

Using (3-11), T-parameter of input and output hybrids are given by:

$$[T]_{IP\ Hybrid} = \begin{bmatrix} \frac{-j}{\sqrt{2}} & \frac{-1}{\sqrt{2}} & 0 & 0 \\ \frac{-1}{\sqrt{2}} & \frac{-j}{\sqrt{2}} & 0 & 0 \\ \frac{-j(K_i - 1)}{\sqrt{2}(K_i + 1)} & \frac{(K_i - 1)}{\sqrt{2}(K_i + 1)} & \frac{j}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ \frac{(K_i - 1)}{\sqrt{2}(K_i + 1)} & \frac{-j(K_i - 1)}{\sqrt{2}(K_i + 1)} & \frac{-1}{\sqrt{2}} & \frac{j}{\sqrt{2}} \end{bmatrix} \tag{3.28}$$

$$[T]_{OP\ Hybrid} = \begin{bmatrix} \frac{-j}{\sqrt{2}} & \frac{-1}{\sqrt{2}} & \frac{j(K_0 - 1)}{\sqrt{2}(K_0 + 1)} & \frac{-(K_0 - 1)}{\sqrt{2}(K_0 + 1)} \\ \frac{-1}{\sqrt{2}} & \frac{-j}{\sqrt{2}} & \frac{-(K_0 - 1)}{\sqrt{2}(K_0 + 1)} & \frac{j(K_0 - 1)}{\sqrt{2}(K_0 + 1)} \\ 0 & 0 & \frac{j}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ 0 & 0 & \frac{-1}{\sqrt{2}} & \frac{j}{\sqrt{2}} \end{bmatrix} \tag{3.29}$$

Using (3-12), the four quadrants, $[T_{I,I}], [T_{I,II}][T_{II,I}], [T_{II,II}]$, of cascaded T-parameter are calculated and are given in (3-30), (3-31), (3-32) and (3-33).

$$[T_{I,I}]_{Cascaded} = \begin{bmatrix} 0 & j\left(1-\frac{Z_0}{2Z}\right) \\ j\left(1-\frac{Z_0}{2Z}\right) & 0 \end{bmatrix} \tag{3.30}$$

$$[T_{I,II}]_{Cascaded} = \begin{bmatrix} -\frac{Z_0}{2Z}+\left(\frac{K_0-1}{K_0+1}\right)\left(1-\frac{Z_0}{2Z}\right) & 0 \\ 0 & -\frac{Z_0}{2Z}+\left(\frac{K_0-1}{K_0+1}\right)\left(1-\frac{Z_0}{2Z}\right) \end{bmatrix} \tag{3.31}$$

$$[T_{II,I}]_{Cascaded} = \begin{bmatrix} \frac{Z_0}{2Z}-\left(\frac{K_i-1}{K_i+1}\right)\left(1-\frac{Z_0}{2Z}\right) & 0 \\ 0 & \frac{Z_0}{2Z}+\left(\frac{K_i-1}{K_i+1}\right)\left(1-\frac{Z_0}{2Z}\right) \end{bmatrix} \tag{3.32}$$

$$[T_{II,II}]_{Cascaded} = \begin{bmatrix} 0 & C \\ C & 0 \end{bmatrix} \tag{3.33}$$

where $C = -j\left(\frac{2Z+Z_0}{2Z}\right) - j\left(\frac{K_i-1}{K_i+1}+\frac{K_0-1}{K_0+1}\right)\frac{Z_0}{2Z} + j\left(\left(\frac{K_i-1}{K_i+1}\right)\left(\frac{K_0-1}{K_0+1}\right)\right)\left(1-\frac{Z_0}{2Z}\right)$.

Using (3-13), S-parameter of the cascaded network is obtained from its T-parameter. The four quadrants of S-parameter of the cascaded network is given by:

$$[S_{I,I}]_{Cascaded} = \begin{bmatrix} 0 & j\frac{(K_0-K_i)Z-K_0K_iZ_0}{(K_0+K_i)Z+K_0K_iZ_0} \\ j\frac{(K_0-K_i)Z-K_0K_iZ_0}{(K_0+K_i)Z+K_0K_iZ_0} & 0 \end{bmatrix} \tag{3.34}$$

$$[S_{I,II}]_{Cascaded} = \begin{bmatrix} 0 & j\frac{2\sqrt{K_0K_i}Z}{(K_0+K_i)Z+K_0K_iZ_0} \\ j\frac{2\sqrt{K_0K_i}Z}{(K_0+K_i)Z+K_0K_iZ_0} & 0 \end{bmatrix} \tag{3.35}$$

$$[S_{II,I}]_{Cascaded} = \begin{bmatrix} 0 & j\frac{2\sqrt{K_0K_i}Z}{(K_0+K_i)Z+K_0K_iZ_0} \\ j\frac{2\sqrt{K_0K_i}Z}{(K_0+K_i)Z+K_0K_iZ_0} & 0 \end{bmatrix} \tag{3.36}$$

$$[S_{II,II}]_{Cascaded} = \begin{bmatrix} 0 & j\frac{(K_0-K_i)Z-K_0K_iZ_0}{(K_0+K_i)Z+K_0K_iZ_0} \\ j\frac{(K_0-K_i)Z-K_0K_iZ_0}{(K_0+K_i)Z+K_0K_iZ_0} & 0 \end{bmatrix} \tag{3.37}$$

$$[S] = \begin{bmatrix} 0 & j\frac{(k_0 - k_i)Z - k_0 k_i Z_0}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 & j\frac{2\sqrt{k_0 k_i}Z}{(k_0 + k_i)Z + k_0 k_i Z_0} \\ j\frac{(k_0 - k_i)Z - k_0 k_i Z_0}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 & j\frac{2\sqrt{k_0 k_i}Z}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 \\ 0 & j\frac{2\sqrt{k_0 k_i}Z}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 & j\frac{(k_0 - k_i)Z - k_0 k_i Z_0}{(k_0 + k_i)Z + k_0 k_i Z_0} \\ j\frac{2\sqrt{k_0 k_i}Z}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 & j\frac{(k_0 - k_i)Z - k_0 k_i Z_0}{(k_0 + k_i)Z + k_0 k_i Z_0} & 0 \end{bmatrix} \quad (3.38)$$

From (3-38), insertion loss and isolation port transmission coefficient of complete T/R switch are given by:

$$Receive\ Path\ Loss = |S_{41}| = \left|\frac{2\sqrt{K_0 K_i}Z}{(K_0 + K_i)Z + K_0 K_i Z_0}\right| \quad (3.39)$$

$$Transmit\ Path\ Loss\ = |S_{21}| = \left|\frac{(K_0 - K_i)Z - K_0 K_i Z_0}{(K_0 + K_i)Z + K_0 K_i Z_0}\right| \quad (3.40)$$

Both of which reduce to (3.20) and (3.21) when $K_i = K_0 = 1$. Fig. 3-14 shows the variation in insertion loss *w.r.t.* impedance transforming ratio when the switch is in 'OFF' state and its impedance is assumed to be 1000 Ω. Similarly, Fig. 3-15 shows the variation in isolation port transmission coefficient when the switch is in 'ON' state and its impedance is assumed to be 1 Ω.

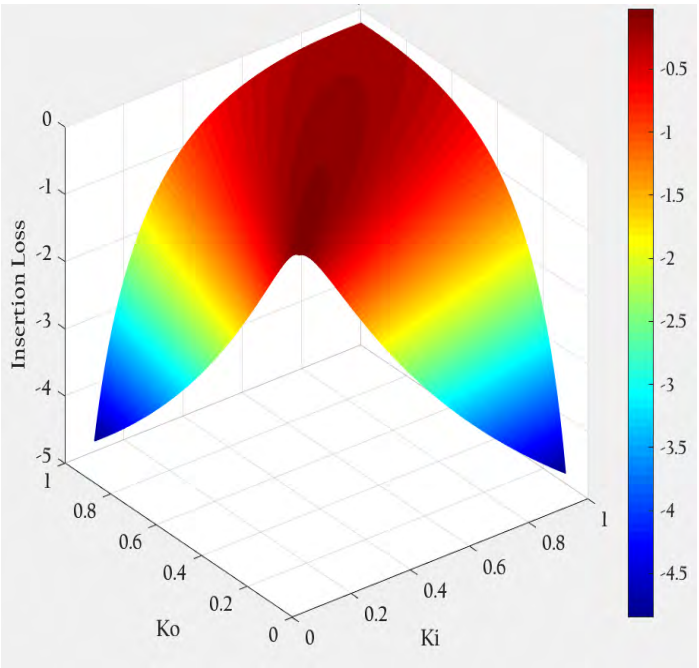


Figure 3-14. Insertion loss variation of switch *w.r.t.* K_i, K_0 when shunt FET is 'off' and Z =1000Ω

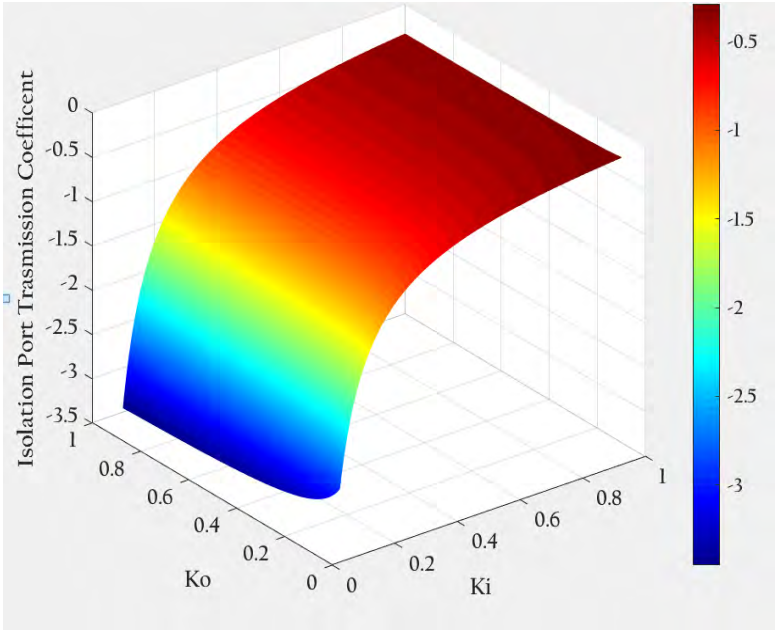


Figure 3-15. Isolation port transmission coefficient variation of switch w.r.t. K_i, K_0 when shunt FET is 'on' and Z =1Ω

Revisiting the case of 200W GaN T/R switch, with the new *impedance transformation with on-the-chip coherent current distribution technique*, from (3.6), (3-39) and (3-40), for step down transformation from 50Ω to 25Ω, i.e., $K_i = K_0$ =0.5, Fig. 3-16 and Fig. 3-17 show the modified receive path and transmit path performances.

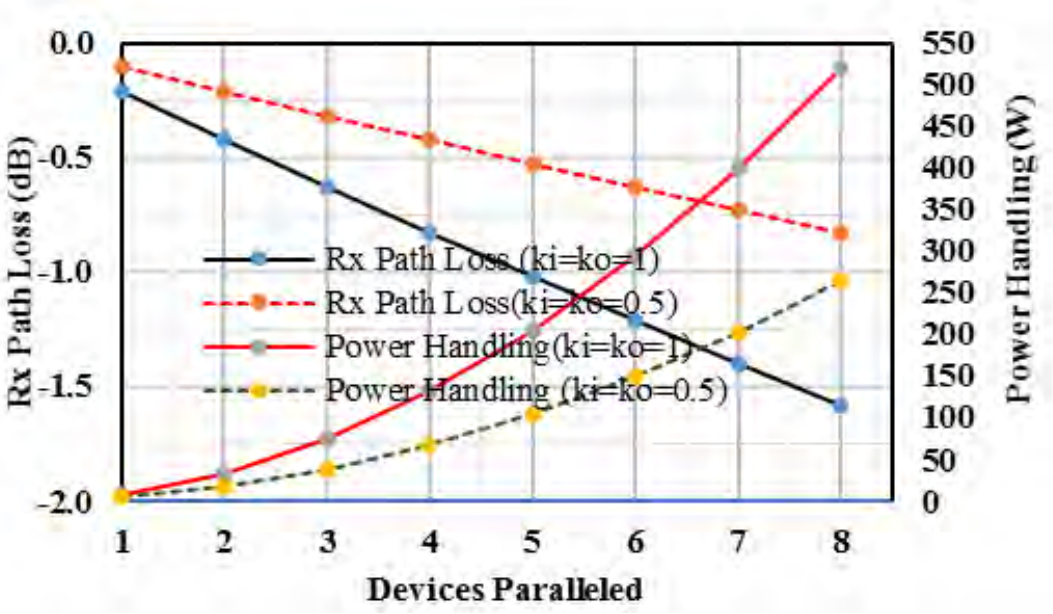


Figure 3-16. Maximum power handling capability of GaN T/R Switch (GH25- UMS) and Receive path loss as a function of no. of devices paralleled, with and without impedance transformation

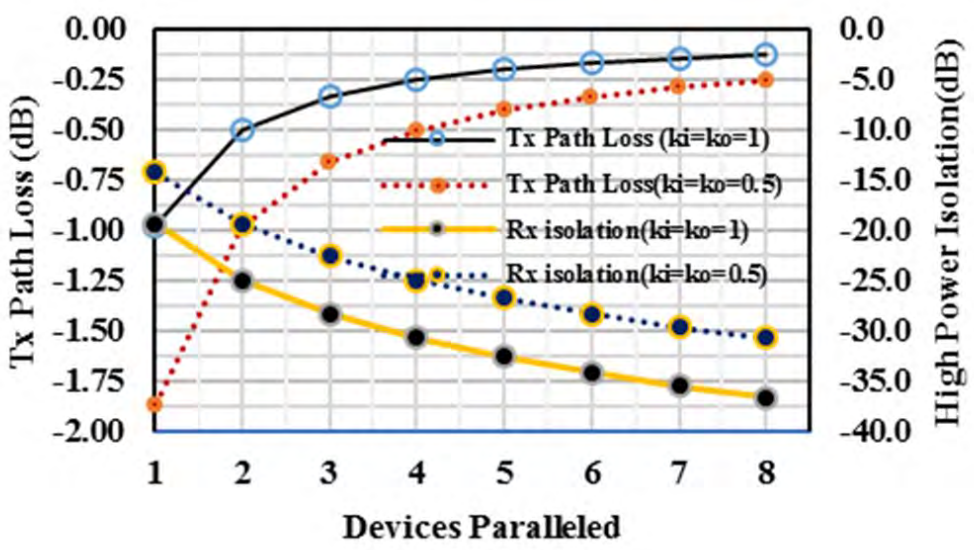


Figure 3-17. Transmit path loss and Receive path isolation as a function of no. of devices paralleled, with and without impedance transformation, of GaN T/R Switch (GH25- UMS)

It can be seen from Fig. 3-16, the 50Ω to 25Ω transformation improves receive loss by 0.8 dB, with only 3dB reduction in power handling, which otherwise would have been 6 dB if half the no. of devices are paralleled. In addition to the improved receive path loss, the impedance transformation technique provides reduced voltage swing across FET, a desirable condition to have as the switch is handling large RF power.

By employing the step-down impedance transformation technique, along with coherent current distribution across 8 identical devices, it can be seen from Fig. 3-16 and Fig. 3-17, a 3.1 W power handling capable GaN FET device is employed to realize a 260 W T/R Switch having transmit loss of 0.25 dB with receive isolation of 30 dB and receive path loss of 0.8 dB, with ideal loss less hybrids.

3.2.4 High power T/R switch employing FET stacking technique and on-the-chip coherent current distribution technique

Designing a GaAs high power T/R switch, which is to be used as a Receive protection switch, conventionally a PIN diode based switch, while the Transmit/Receive functionality is addressed by a Ferrite circulator, as shown in Fig. 1-1., is examined in case-3. *For application as a receive protection switch, the receive path loss needs to be minimized, maintaining the higher power handling capability.*

3.2.4.1 Case -3: 20W Receive Protection Switch using 0.13µm GaAs pHEMT (D01PHS-M/s OMMIC)

The chosen, OMMIC-D01PHS low noise process has typical parameters like V_p=-0.9V, $V_{DS\ max}$=8V, I_{DSS} typ.=500mA/mm. The largest characterized gate periphery offered by the process is 600 µm (8x75µm), whose R_{DSON} and $R_{DS\ OFF}$ are 2.0 and 600Ω, respectively. This process, in the conventional configuration, yields a unit cell switch with **Pmax, of 0.6W** in low impedance state. The maximum power handling capability T/R switch, transmit path and the receive path losses, receive isolation of complete T/R switch, as a function of number of devices paralleled, calculated using equations (3.18) and (3.19) for the typical process chosen, with ideal input and output hybrids, and is given in the following Fig. 3-18 and Fig. 3-19.

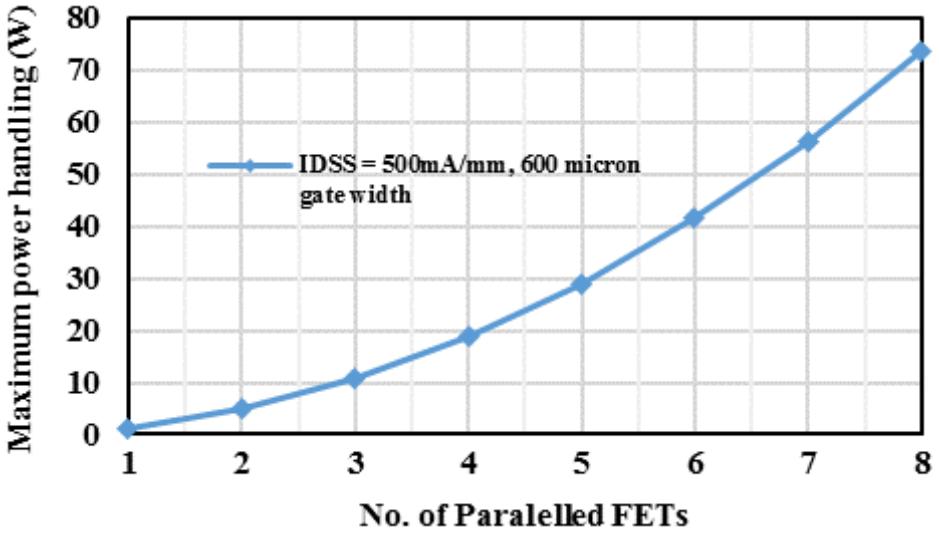


Figure 3-18. Maximum power handling capability of GaAs T/R Switch (D01PHS-OMMIC) as a function of no. of devices paralleled.

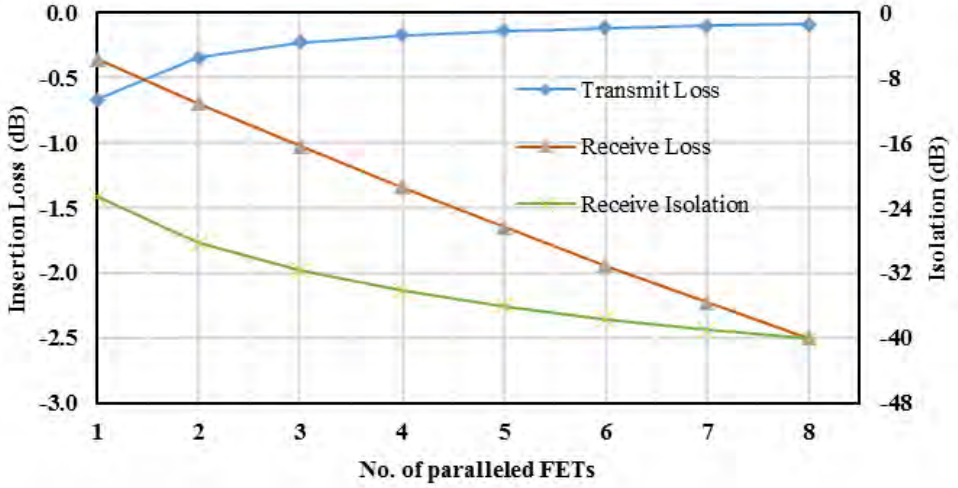


Figure 3-19. Performance T/R Switch performance as a function of no. of devices paralleled

As can be seen from Fig. 3-18 and Fig. 3-19, a 600mW power handling capable FET device is employed to realize a 20W T/R Switch, with coherent current distribution across 4 identical devices, having transmit loss of 0.17 dB with receive isolation of 34 dB and receive loss of 1.34 dB. Receive path loss can be reduced by reducing the no. of FETs paralleled but the power handling capability reduces significantly. Hence another novel technique viz., *FET Stacking with On-the-chip coherent Current distribution*, is proposed to improve Receive path loss without affecting the power handling capability of the T/R switch.

3.2.4.2 FET Stacking with On-the-chip coherent Current distribution

FET stacking is generally employed to increase the power handling capability in high impedance state [8], extending and modifying the work of Shifrin et.al., [8], but in the present work, FET stacking is used to increase the R_{DSOFF} to improve the low power receive path loss, while power handling capability is achieved by on-the-chip coherent current paralleling. Fig. 3-20 shows the schematic of interconnect compensated, stacked and current paralleled high power T/R Switch.

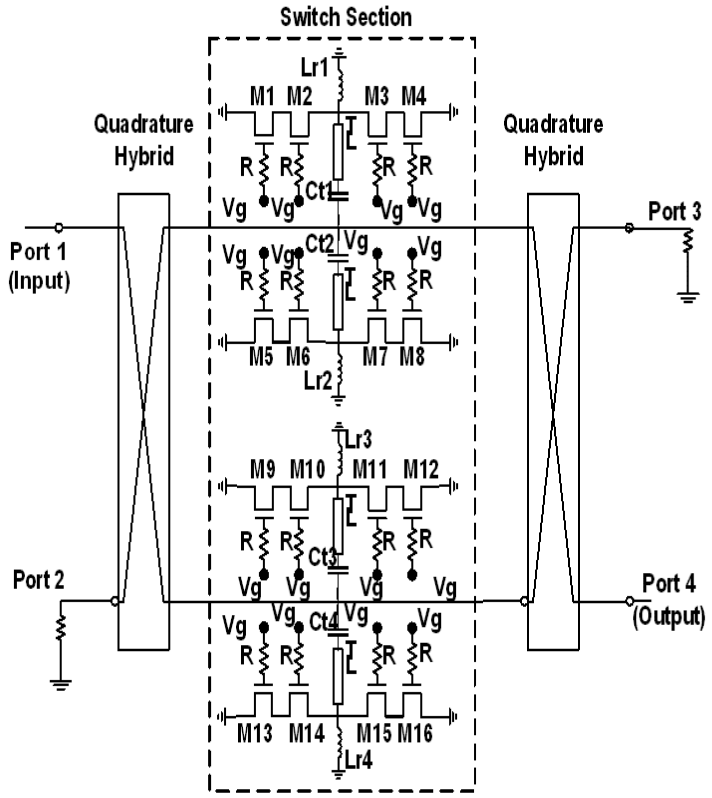


Figure 3-20. Schematic of interconnect compensated, stacked and current paralleled high power T/R Switch

The upper high power switch section is made up of M1 to M8 FETs connected in *resonant shunt stacked FET configuration*. In resonant FET configuration, a shunt inductor, Lr, connected across drain and source terminals is used to parallel resonate the drain-source capacitance, C_{DS}. An exactly identical switch section made up of FETs M9 to M16 is used in the lower branch of the quadrature hybrid. During high power transmission, with gate control, Vg ≥ 0V, all the switching FETs viz., M1 to M8 and M9 to M16 are "ON", offering low shunt impedance, and so the high input power fed from Port1 is reflected from the both the switches and gets added constructively at Port2. Port 2 is connected to an off-chip high power termination, thus creating an absorptive protection switch. While, during low power reception, with gate control, Vg ≤ pinch off voltage, Vp, all the switching FETs viz., M1 to M8 and M9 to M16 are "OFF", offering large shunt impedance, and so power fed from Port 1 is routed to the input of both LNAs. Here, each of the current paralleled branches contains 2 stacked FETs of identical periphery, in place of one FET in each branch, as shown in Fig. 3-5. Hence, as the number of branches are not reduced, the power handling capability remains same, but due to doubling of $R_{DS\ OFF\ eff}$ because of 2 FETs connected in series, the receive path loss reduces. The transmit path and the receive path losses as a function of no. of devices paralleled, are calculated by using equations (3.20) and (3.21) for D01PHS device, with ideal input and output hybrids, for the cases of paralleled single FETs and paralleled 2 FET stack and are shown following Fig. 3-21.

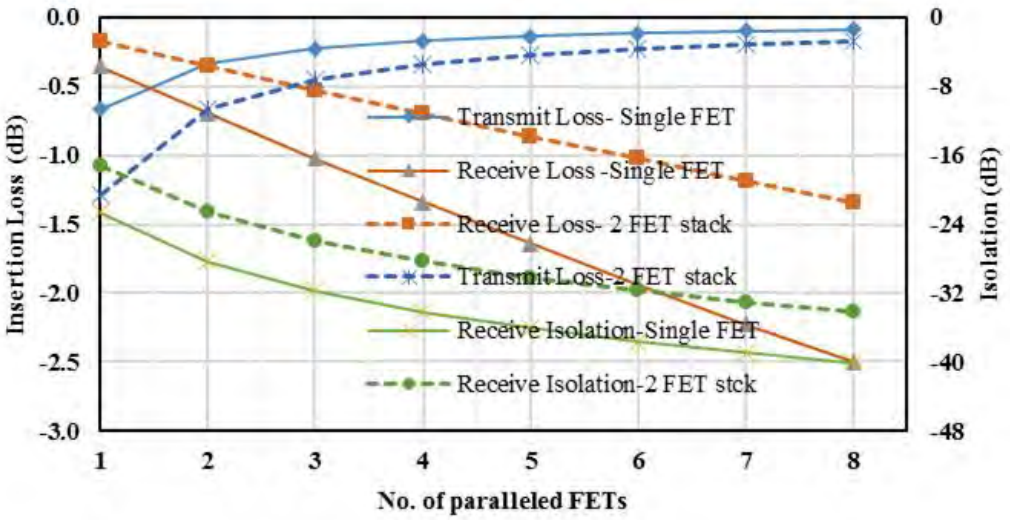


Figure 3-21. Receive protection Switch performance as a function of no. of devices paralleled, with and without FET Stacking

Due to FET stacking, slight degradation in high power transmit path loss and receive isolation are expected because of the increase in the R_{DSON}. **As can be seen from Fig. 3-21, with FET stacking and current paralleling, the protection switch can give 0.7 dB improved low power receive path loss while maintaining power handling capability of around 18.5W.** Also, due to this 2-FET stacking, the power handling capability in receive mode increases by 6 dB [2] compared to the single FET switch.

3.3 Realization and Validation Approach

To validate the techniques described in the earlier section, design and fabrication and experimental validation of (a) 10W GaAs T/R switch with LNA and (b) 20W GaAs receive protection switch with LNA has been carried out. Circuit and layout level electromagnetic co-simulations are presented for (c) a 200W GaN T/R switch with LNA.

To this extent, all the constituent high power MMIC quadrature hybrids, high power T/R switches, LNAs and integrated high power switch and LNA MMICs are designed. Subsequent chapters present design, simulation and measurement/characterization results of each of the above circuit elements.

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Chapter: 4

Quadrature Hybrids

4.1 Introduction

Quadrature hybrids are 3-dB directional coupler with a 90° phase difference between its two output ports. Fig. 4-1 shows schematic of a quadrature hybrid.

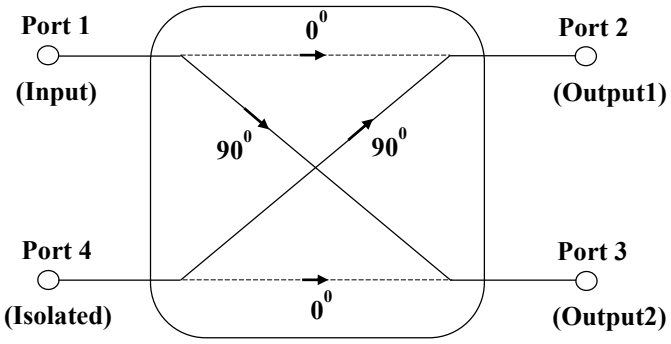


Figure 4-1. Schematic of quadrature hybrid

The S-parameter of a quadrature hybrid shown in Fig. 4-1 is given by:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{4.1}$$

Port 4 is isolated w.r.t. input port 1. Any reflection due to mismatch at the output ports are absorbed in matched load at port 4. Since quadrature hybrids are generally symmetrical network, any port can be used as input port and functions of other ports are appropriately assigned. This symmetry is reflected in its scattering matrix (4.1), as

each row is transposition of the first row. Analysis of quadrature hybrids follows even-mode and odd-mode approach, as shown in Fig. 4-2 [1].

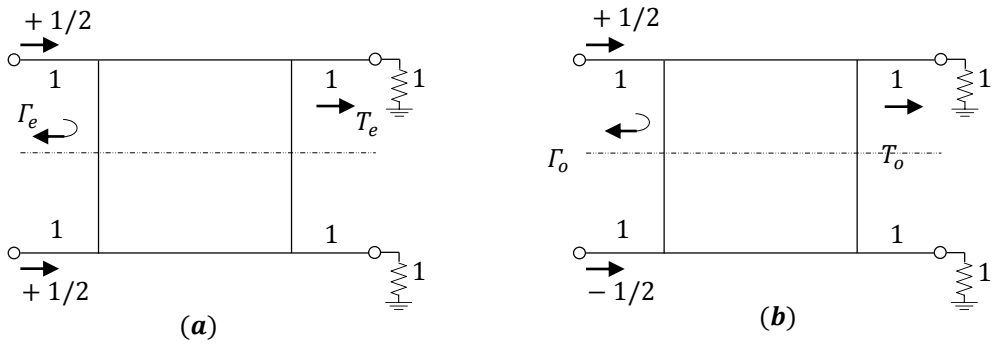


Figure 4-2. (a) Even mode and (b) odd mode excitation of quadrature hybrid.

Superposition of these two sets of excitation, even mode and odd mode, generates a unit amplitude voltage wave incident at port 1. Emerging wave at each port of quadrature hybrid is given as:

$$b_1 = \frac{1}{2}\Gamma_e + \frac{1}{2}\Gamma_0 \tag{4.2}$$

$$b_2 = \frac{1}{2}T_e + \frac{1}{2}T_0 \tag{4.3}$$

$$b_3 = \frac{1}{2}T_e - \frac{1}{2}T_0 \tag{4.4}$$

$$b_4 = \frac{1}{2}\Gamma_e - \frac{1}{2}\Gamma_0 \tag{4.5}$$

where b_1, b_2, b_3 and b_4 are outgoing waves from port 1, 2 , 3 and 4 respectively. Due to symmetry and anti-symmetry of even and odd mode excitation, four port network is decomposed into two port network. $\Gamma_{e,0}$ and $T_{e,o}$ are even and odd mode reflection and transmission coefficients of decomposed two port network. Chain matrix of the decomposed two port network is derived which is then converted to S-parameter as given below:

$$\Gamma = \frac{A + B - C - D}{A + B + C + D} \tag{4.6}$$

$$T = \frac{2}{A + B + C + D} \tag{4.7}$$

where $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$ is the chain matrix of decomposed two port network. $\Gamma_{e,0}$ and $T_{e,o}$ computed from (4.6)-(4.7) is substituted in (4.2)-(4.5) to obtain the first row of 4 port S-parameter of quadrature hybrid. As the hybrid is symmetric, remaining rows of S-parameter matrix is obtained by transposition of first row.

4.1.1 Applications:

Quadrature hybrids find large application in various RF circuits. They are widely used in voltage variable phase shifters, attenuators, balanced amplifier, frequency discriminator and image-reject mixers. Fig. 4-3 shows schematic of a reflection phase shifter/attenuator. Input signal at port 1 is equally divided between port 2 and 3. Reflection from a voltage variable load, Z_L cancels at port 1 and combines at output port 4. If the variable loads are varactor diode, change in its bias voltage changes the phase of reflection coefficient, thus realizing a voltage variable phase shifter. If varactor are replaced with PIN diodes, then bias current variation results in current variable attenuator.

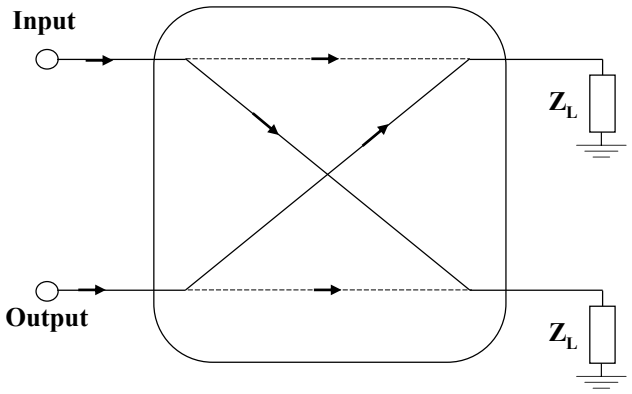


Figure 4-3. Schematic of reflection phase shifter/attenuator

Fig. 4-4 shows schematic of a balanced amplifier using quadrature hybrid at its input and output. Input and output reflection from both amplifiers are combined at input and output hybrid isolation termination, thus providing a very low reflection coefficient at both input and output ports.

Various mixer circuits use quadrature hybrids to suppress the image signal and unwanted sidebands. Fig. 4.5 shows a single balanced mixer circuit, where quadrature hybrid provides large isolation between LO and RF signals. Due to orientation of

diodes, sum frequency of the mixing product is shorted whereas difference frequency (intermediate frequency) is transmitted to output.

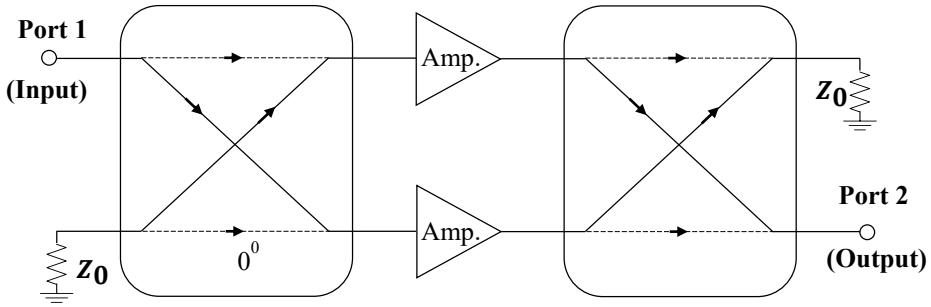


Figure 4-4. Schematic of balanced amplifier

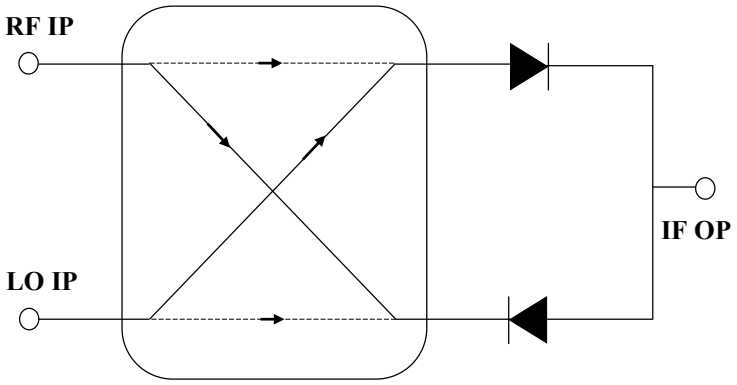


Figure 4-5. Schematic of single balanced mixer

4.1.2 Errors in Quadrature Hybrid

Practical quadrature hybrid circuit has errors in amplitude and quadrature phase balance over intended bandwidth of operation. Effect of amplitude and quadrature imbalance on the performance of circuit, where quadrature hybrid is used, is required. Fig. 4-6 shows vector analysis of an imperfect quadrature hybrid. $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ are output vectors with phase imbalance of $\alpha_1 + \alpha_2$. Each of these two vectors is resolved such that one component pair has equal amplitude and quadrature phase whereas other component pair (magnitude $= r$ and relative angle $= \theta$) denotes the error in quadrature hybrid. If $\theta = 0^0$, hybrid has only imbalance in amplitude whereas if $\theta = 90^0$, hybrid has only phase imbalance. Error quantity of interest, r, after some mathematical

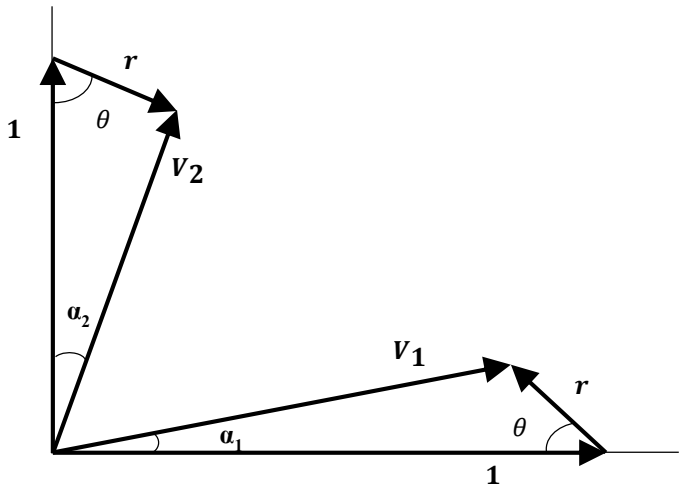


Figure 4-6. Analysis of quadrature hybrid error

manipulation is given by:

$$\frac{1}{2}\left(\frac{v_1}{v_2}+\frac{v_2}{v_1}\right)\sec\alpha = \frac{1+r^2}{1-r^2} \tag{4.8}$$

A graphical interpretation of (4.8) can be obtained from:

$$x = \sqrt{\log\left[\frac{1}{2}\left(\frac{v_1}{v_2}+\frac{v_2}{v_1}\right)\right]} \tag{4.9}$$

$$y = \sqrt{\sec\alpha} \tag{4.10}$$

$$R = \sqrt{\log\left(\frac{1+r^2}{1-r^2}\right)} \tag{4.11}$$

$$R^2 = x^2 + y^2 \tag{4.12}$$

Relationship between amplitude and phase imbalance and error magnitude, r is a circular contour. This graphical representation is useful in various analysis of practical circuits employing quadrature hybrid. For example, in a balanced amplifier, as shown in Fig. 4-4, the magnitude of r is ratio of voltage wave *w.r.t* input voltage wave arriving at isolation termination.

4.2 Types of Quadrature Hybrid

Quadrature hybrids are designed either in distributed or lumped configuration depending upon frequency of operation, size of hybrid and type of circuit

(MIC/MMIC). Distributed design approach, for example parallel coupled line, Lange coupler, branch-line hybrid, are bulky in size and are not suitable for MMIC whereas lumped circuit design approach are compact in size but has narrower bandwidth. The following section provides a brief of various types of quadrature hybrids used in present work.

4.2.1 Via-less Lumped Element Hybrid

Conventional lumped element hybrid requires many via holes for grounding shunt components. Hou and Wang have reported a via less quadrature hybrid, which is based on high-pass and low-pass lumped element topology [4]. Fig. 4-7 shows the schematic of via-less lumped element quadrature hybrid. As this hybrid does not require bulky via holes, they are more compact in size. Moreover, it also provides a wider bandwidth and better matching and isolation. S-parameter of the via-less quadrature hybrid is given by equation (4.13). Fig. 4-8 shows the even and odd mode

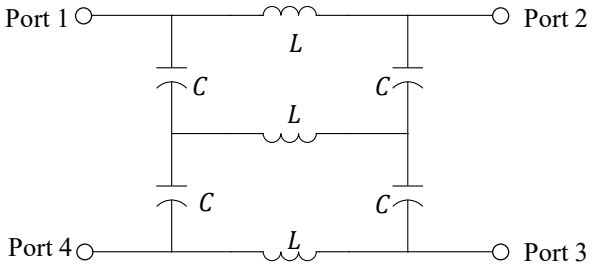


Figure 4-7. Schematic of via-less lumped element quadrature

decomposed equivalent circuit. Even mode and odd mode chain matrix is given by equation (4.14) and (4.15) respectively.

$$[S] = \begin{bmatrix} 0 & \frac{1-j}{2} & \frac{1+j}{2} & 0 \\ \frac{1-j}{2} & 0 & 0 & \frac{1+j}{2} \\ \frac{1+j}{2} & 0 & 0 & \frac{1-j}{2} \\ 0 & \frac{1+j}{2} & \frac{1-j}{2} & 0 \end{bmatrix} \tag{4.13}$$

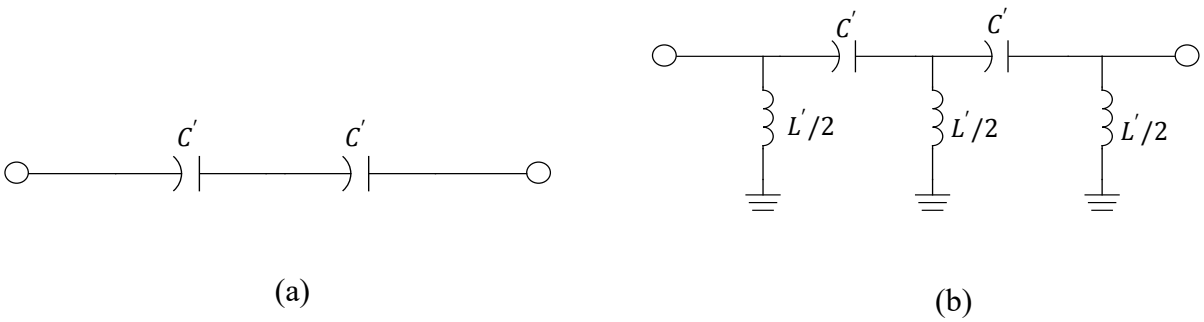


Figure 4-8. Even and odd mode equivalent circuit of via-less lumped hybrid. (a): Even mode (b): Odd mode

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} 1 & \frac{-j2}{\omega C'} \\ 0 & 1 \end{bmatrix} \tag{4.14}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_0 = \begin{bmatrix} 1 - \frac{1}{\omega^2 L'C'}\left(6 - \frac{4}{\omega^2 L'C'}\right) & \frac{-j2}{\omega C'}\left(1 - \frac{4}{\omega^2 L'C'}\right) \\ \frac{-j6}{\omega L'} + \frac{j8}{\omega^3 L'^2 C'}\left(2 - \frac{1}{\omega^2 L'C'}\right) & 1 - \frac{1}{\omega^2 L'C'}\left(6 - \frac{4}{\omega^2 L'C'}\right) \end{bmatrix} \tag{4.15}$$

where L' and C' are normalized inductance and capacitance *w.r.t.* characteristic impedance, Z_0. From equation (4.2) – (4.7), lumped element L and C are given by:

$$L = \frac{Z_0}{\omega} \tag{4.16}$$

$$C = \frac{1}{\omega Z_0} \tag{4.17}$$

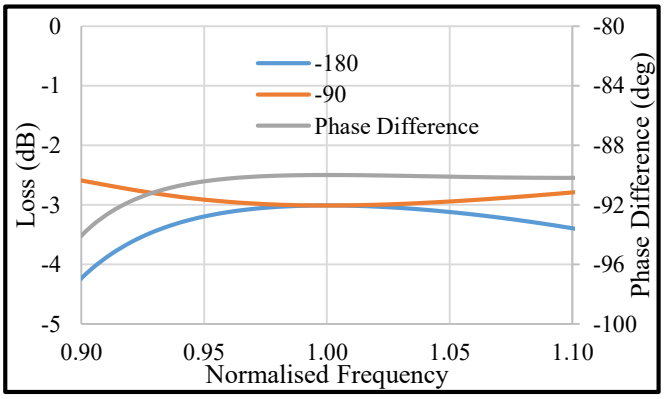


Figure 4-9. Insertion and coupled path response of via-less quadrature hybrid.

Fig. 4-9 shows the response of via-less lumped element quadrature hybrid.

4.2.2 Quasi Lumped Element Quadrature Hybrid

Lumped element quadrature hybrid implemented in MMIC cannot be used in high power applications due to limited current handling capability of the inductor. Inductor less quasi lumped element quadrature hybrid uses distributed transmission line in series arm and capacitive coupling in shunt arm as shown in Fig. 4-10. As the power handling capability of wider width transmission line and lumped capacitor is higher than spiral inductors, this topology is used in high power applications. As the network shown in Fig. 4-10 is symmetric, odd and even mode analysis is done to evaluate its element

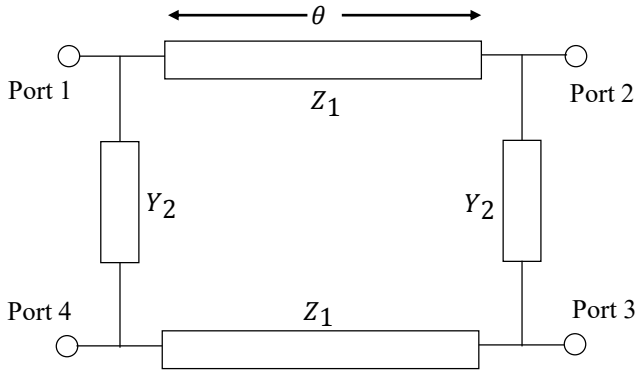


Figure 4-10. Schematic of quasi-lumped element quadrature hybrid

values. Figure 4.11 shows the decomposed two port even and odd mode network where

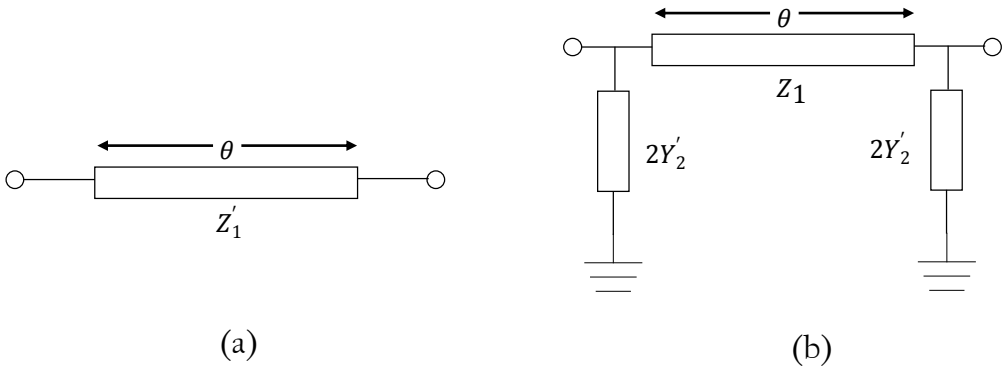


Figure 4-11. Equivalent circuit of quasi-lumped element quadrature hybrid. (a): Even mode (b): Odd mode

$Z_1'$and Y_2' are normalized series arm impedance and shunt arm admittance *w.r.t.* characteristic impedance, Z_0.

Even mode and odd mode chain matrix are given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} \cos\theta_1 & jZ_1' \sin\theta_1 \\ \frac{j}{Z_1'} \sin\theta_1 & \cos\theta_1 \end{bmatrix} \tag{4.18}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_0 =$$

$$\begin{bmatrix} \cos\theta_1 - 2Y_2'Z_1' \sin\theta_1 & jZ_1' \sin\theta_1 \\ 2jY_2' \cos\theta_1 + \frac{j}{Z_1'} \sin\theta_1 + 2jY_2'(\cos\theta_1 - 2Y_2Z_1' \sin\theta_1) & \cos\theta_1 - 2jY_2'Z_1' \sin\theta_1 \end{bmatrix} \tag{4.19}$$

Using equation (4.2) – (4.7) and (4.18) and (4.19), for 3 dB capacitive coupled quasi-lumped quadrature hybrid, element values are given by:

$$Z_1 = Z_0 \tag{4.20}$$

$$\theta_1 = 45^0 \tag{4.21}$$

$$Y_2 = \frac{j}{Z_0} \tag{4.22}$$

Fig. 4-12 shows the through port and coupled port response of quasi-lumped element hybrid.

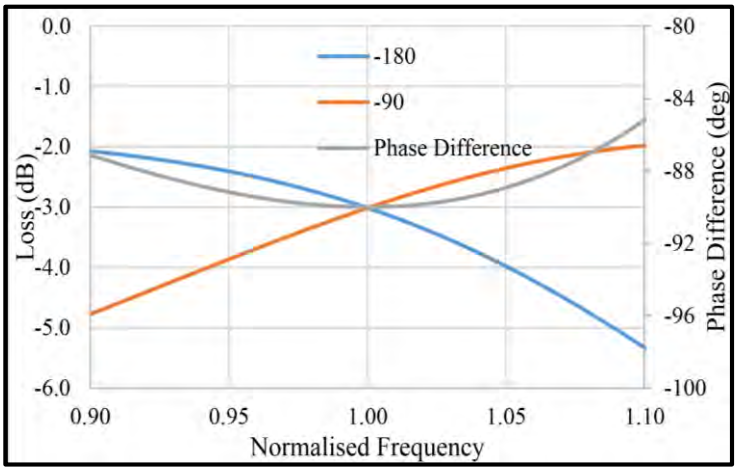


Figure 4-12. Insertion and coupled path response of quasi-lumped element quadrature hybrid

4.2.3 Compact Wide-Band Spiral Quadrature Hybrid

Via-less lumped element quadrature hybrid of the previous sub-section has fractional bandwidth of ~20%. Applications that requires greater than octave bandwidth quadrature hybrid generally employ Lange coupler or multi-section parallel coupler line or branch-line coupler. As these distributed topologies are extremely large in size due to $\lambda/4$ length of transmission lines, it cannot be used in broadband circuits where the size of the circuit is at a premium. Ali has proposed a compact and greater than octave bandwidth spiral monolithic quadrature hybrid [5].

Fig. 4.13 shows the schematic of a monolithic spiral hybrid and its equivalent circuit. It consists of lumped spiral inductor. Mutual coupling of inductor is realized by sandwiching the two multi-turn spiral inductor with inner and outer windings. In Fig. 4.13 Port 1 is designated as input port, Port 2 as coupled port, Port 3 as transmitted port and Port 4 as isolated port. As it is a symmetrical network, any port can be used an input port and the other ports are then defined accordingly.

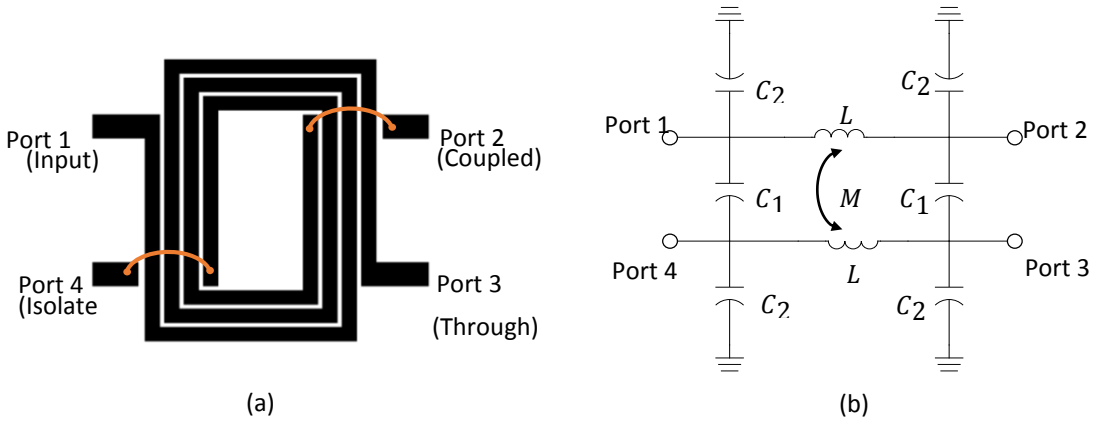


Figure 4-13. Compact wide-band spiral quadrature hybrid (a): Schematic (b): Equivalent Circuit

Equation (4.24) defines the S-parameter of spiral quadrature hybrid with Z_{0e} and Z_{00} as even and odd mode characteristic impedance. As the coupler is symmetric, its analysis follows the odd and even mode excitation approach. For even-mode excitation, unity voltages are applied to ports 1 and 4 while ports 2 and 3 are terminated with characteristic impedance Z_0. For odd-mode excitation, unity voltages of opposite phase are applied at ports 1 and 4 while ports 2 and 3 are terminated with Z_0. Fig. 4-14 shows

the decomposed even and odd mode equivalent circuit of spiral quadrature hybrid. Even mode and odd mode chain matrix are given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} 1-\omega^2 C_2(L+M) & j\omega(L+M) \\ j\omega C_2\left(2-\omega^2 C_2(L-M)\right) & 1-\omega^2 C_2(L+M) \end{bmatrix} \tag{4.23}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_0 = \begin{bmatrix} 1-\omega^2(C_2+C_1)(L-M) & j\omega(L-M) \\ j\omega(C_2+C_1)\left(2-\omega^2(L-M)(C_2+C_1)\right) & 1-\omega^2(L-M)(C_2+C_1) \end{bmatrix} \tag{4.24}$$

$$[S] = \begin{bmatrix} 0 & -j\sqrt{1-\left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right)^2} & \left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right) & 0 \\ -j\sqrt{1-\left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right)^2} & 0 & 0 & \left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right) \\ \left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right) & 0 & 0 & -j\sqrt{1-\left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right)^2} \\ 0 & \left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right) & -j\sqrt{1-\left(\frac{Z_{0e}-Z_{00}}{Z_{0e}-Z_{00}}\right)^2} & 0 \end{bmatrix} \tag{4.25}$$

Using equation (4.2) – (4.7), equivalent lumped element values are given by:

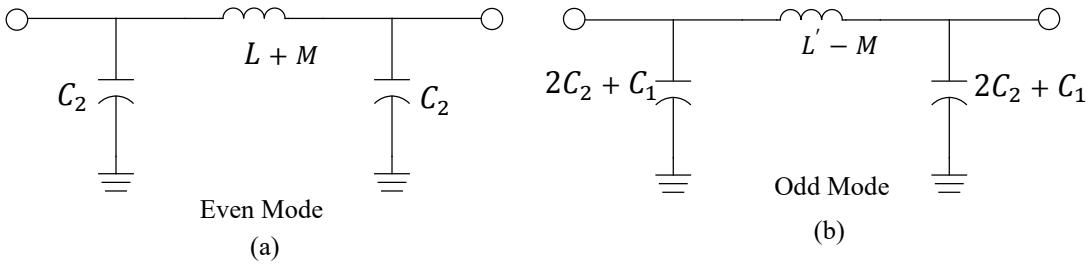


Figure 4-14. Even and odd mode equivalent circuit of spiral quadrature hybrid. (a): Even mode (b): Odd mode

$$L = \frac{0.5(Z_{0e}+Z_{00})}{\omega} \tag{4.26}$$

$$M = \frac{0.5(Z_{0e} - Z_{00})}{\omega} \tag{4.27}$$

$$C_1 = \frac{0.5(Z_{0e} - Z_{00})}{\omega Z_{0e} Z_{00}} \tag{4.28}$$

$$C_2 = \frac{1}{\omega Z_{0e}} \tag{4.29}$$

For 3 dB hybrid, $Z_{00} = (\sqrt{2} - 1)Z_0$ and $Z_{0e} = (\sqrt{2} + 1)Z_0$. Substituting this in equation (4.25) – (4.28), the equivalent lumped element values are given by:

$$L = \frac{\sqrt{2}Z_0}{\omega} \tag{4.30}$$

$$M = \frac{Z_0}{\omega} \tag{4.31}$$

$$C_1 = \frac{1}{\omega Z_0} \tag{4.32}$$

$$C_2 = \frac{(\sqrt{2} - 1)}{\omega Z_0} \tag{4.33}$$

Fig. 4-15 shows the through and coupled path response of 3dB spiral quadrature hybrid. Amplitude imbalance and phase imbalance of better than 0.6dB and 2^0 respectively is obtained over 40% fractional bandwidth. The spiral quadrature hybrid can be implemented in MIC or MMIC configuration using various size of inductor for same operating frequency. Self and mutual inductance calculated using equation (4.29) and equation (4.30) is implemented with a transmission line.

Width of the transmission line determines the current handling capability of the hybrid when the hybrid is used in high power applications. A wider transmission line can be used in higher power application but at the cost of larger size and parasitic capacitance. Hence a trade-off is required while selecting the width of the line such that it meets the power handling requirement in a compact size. As the hybrid is

implemented using sandwiched multi-turn inductors in bifilar configuration, two of its ports require either air-bridge or bond-wire to connect the output pads to internal winding. The air-bridge/bond-wire limits the maximum power handling capability of the hybrid. Electromagnetic simulation of hybrid is required to compensate for the inductance due to air-bridge/bond-wire.

This design approach of quadrature hybrid consumes a considerably smaller amount of GaAs real estate and the chip size is more compact, especially when this kind of coupler has to be integrated with other circuit functions for a multifunction MMIC design.

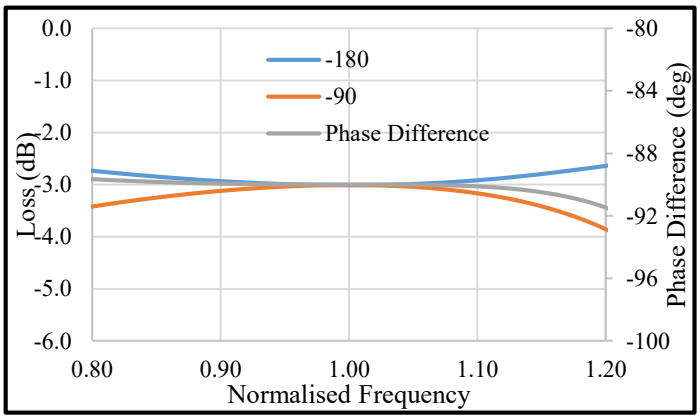


Figure 4-15. Insertion and coupled path response of spiral quadrature hybrid.

4.2.4 Impedance Transforming Quadrature Hybrid

Conventional quadrature hybrid are designed with same input and output characteristic impedance, Z_0. An impedance transforming quadrature hybrid provides

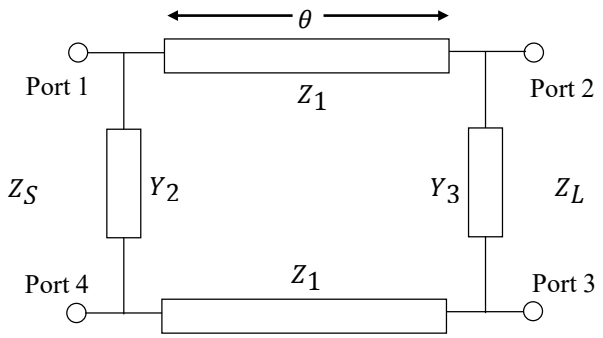


Figure 4-16. Schematic of impedance transforming quasi-lumped element quadrature hybrid

lower/higher value of characteristic impedance at output hence significantly reduces the total number of matching elements required in the design of balanced amplifiers, image reject mixers and reflection phase shifters and attenuators. This class of hybrid provides impedance transformation from incident and isolated port to direct and coupled port [7]. Fig. 4-16 shows the schematic of impedance transforming quasi-lumped element quadrature hybrid.

Z_1 and θ are characteristic impedance and electrical length of through line and Y_2 and

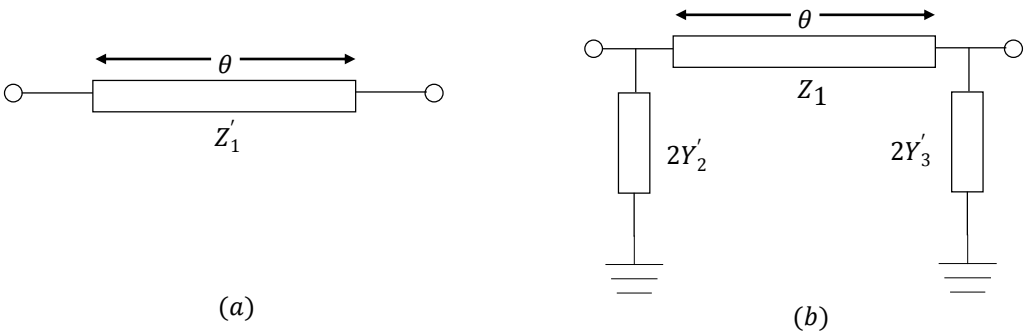


Figure 4.17. Even and odd mode equivalent circuit of impedance transforming hybrid. (a): Even mode (b): Odd mode

Y_3 are shunt admittance in coupled arm at input and output respectively. Z_S and Z_L are source and load impedance respectively, with $Z_S = Z_0$ and $Z_L = KZ_0$, where K is the output impedance transforming ratio. Fig. 4-17 shows the decomposed equivalent circuit for even and odd mode excitation where Z_1', Y_2' and Y_3' are normalized impedance/admittance *w.r.t.* Z_0.

If a two port network is terminated in arbitrary impedances, its voltage and current basis scattering parameter do not satisfy a reciprocal property. Hence, normalized scattering parameters are used for their analysis. Input reflection coefficient, Γ and transmission coefficient, T of two port network with Z_S and Z_L as source and load impedance is given by [8]:

$$\Gamma = \frac{AZ_L + B - CZ_LZ_S - DZ_S}{AZ_L + B + CZ_LZ_S + DZ_S} \tag{4.34}$$

$$T = \frac{2\sqrt{Z_LZ_S}}{AZ_L + B + CZ_LZ_S + DZ_S} \tag{4.35}$$

Γ and T after normalizing *w.r.t.* $Z_S = Z_0$ is given by:

$$\Gamma = \frac{AK + B - CK - D}{AK + B + CK + D} \tag{4.36}$$

$$T = \frac{2\sqrt{K}}{AK + B + CK + D} \tag{4.37}$$

Even and odd mode chain matrix is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} \cos\theta_1 & jZ_1' \sin\theta_1 \\ \frac{j}{Z_1'} \sin\theta_1 & \cos\theta_1 \end{bmatrix} \tag{4.38}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_0 = \begin{bmatrix} \cos\theta_1 - 2Y_3'Z_1' \sin\theta_1 & jZ_1' \sin\theta_1 \\ 2jY_2' \cos\theta_1 + \frac{j}{Z_1'} \sin\theta_1 + 2jY_3'(\cos\theta_1 - 2Y_2'Z_1' \sin\theta_1) & \cos\theta_1 - 2Y_2'Z_1' \sin\theta_1 \end{bmatrix} \tag{4.39}$$

where $Z_1' = Z_1/Z_0$ and $Y_2' = Y_1Z_0$. Using equations (4.2) – (4.5) and equation (4.31) – (4.32) yield the design equation for equal power split, prefect match and isolation.

$$(K - 1)\cos\theta_1 = 0 \tag{4.40}$$

$$\left(Z_1' - \frac{K}{Z_1'}\right)\sin\theta_1 = 0 \tag{4.41}$$

$$Z_1'^2 \sin\theta_1 - \sqrt{2K}\, Z_1' + K \sin\theta_1 = 0 \tag{4.42}$$

$$Y_2' = 1 \tag{4.43}$$

$$Y_3' = \frac{1}{K} \tag{4.44}$$

Design equations (4.40) – (4.44) indicates perfect match and 3dB power split

between output ports of hybrid. As is evident from equations (4.40) – (4.41), if θ_1 =90^0, $Z_1' = \sqrt{K}$, which is not satisfied by equation (4-42). If $\theta_1 \neq 90^0$, then $K = 1$, which implies same input and output characteristic impedances. *Hence perfect match, isolation and equal power split cannot be achieved simultaneously using above topology for impedance transforming quadrature hybrid.*

4.2.5 Modified Impedance Transforming Quadrature Hybrid

To achieve perfect match, isolation and impedance transformation simultaneously in 3dB quasi-lumped element quadrature hybrid, a new topology, as shown in Fig. 4-18 is proposed.

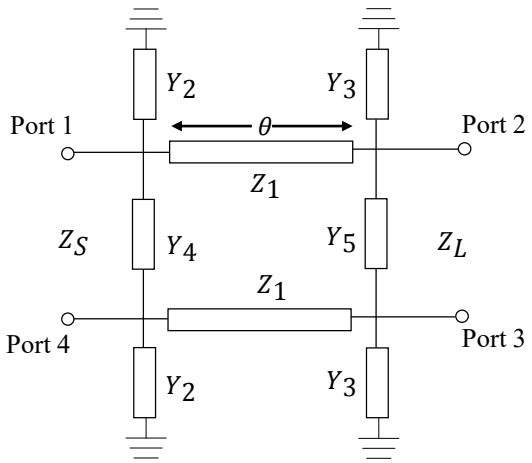


Figure 4-18. Schematic of proposed topology of impedance transforming quadrature hybrid

Z_1 and θ_1 are characteristic impedance and electrical length of through line and Y_2, Y_3, Y_4 and Y_5 are shunt admittance in coupled arm at input and output ports. Due to

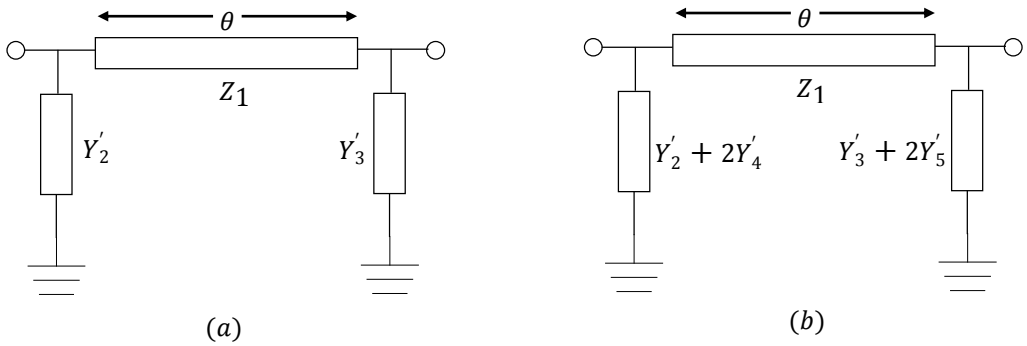


Figure 4.19. Even and odd mode equivalent circuit of proposed topology.

(a): Even mode (b): Odd mode

increase in number of elements in the hybrid, perfect match, isolation and impedance transformation is achieved simultaneously. Figure 4.19 shows the decomposed equivalent circuit for even and odd mode excitation.

Even mode chain matrix is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} \cos\theta_1 - Y_3' Z_1' \sin\theta_1 & jZ_1' \sin\theta_1 \\ jY_2' \cos\theta_1 + \frac{j}{Z_1'} \sin\theta_1 + jY_3'(\cos\theta_1 - Y_2' Z_1' \sin\theta_1) & \cos\theta_1 - Y_2' Z_1' \sin\theta_1 \end{bmatrix} \quad (4.45)$$

where Z_1' is series arm normalized impedance and Y_2', Y_3' are shunt arm normalized admittance. Equation (4.36) – (4.37) and (4.45) yields the following design equations:

$$Z_1' \sin\theta_1 = \sqrt{\frac{K}{2}} \quad (4.46)$$

$$\cos\theta_1 - Y_2' Z_1' \sin\theta_1 = -\sqrt{\frac{K}{2}} \quad (4.47)$$

$$\cos\theta_1 - Y_3' Z_1' \sin\theta_1 = \frac{-1}{\sqrt{2K}} \quad (4.48)$$

$$Y_2' \cos\theta_1 + \frac{\sin\theta_1}{Z_1'} + Y_3'(\cos\theta_1 - Y_2' Z_1' \sin\theta_1) = \frac{1}{\sqrt{2K}} \quad (4.49)$$

From the above analysis, it is evident that the proposed topology of quasi lumped element quadrature hybrid can achieve simultaneous perfect match and impedance transformation. But as (4.46) – (4.48) are not independent system of equations, no unique solution exists. For a desired impedance ratio, K any value of θ can be chosen and subsequently remaining element value Z_1, Y_2 and Y_3 can be derived.

When the proposed topology is to be used in high power application, an inductor less hybrid is desired as a smaller width of inductor and its air-bridge/bond-wire limits the power handling capability of hybrid. For inductor less hybrid, selection of electrical

length of series line, θ is done such that Y_2 and $Y_3 > 0$. Hence from equation (4.42) – (4.43), for inductor less hybrid.

$$\theta_1 > \cos^{-1}\left(\frac{1}{\sqrt{2K}}\right) \qquad for\ 0.5 \ll K \ll 1 \tag{4.50}$$

$$\theta_1 > \cos^{-1}\left(\sqrt{\frac{K}{2}}\right) \qquad for\ 1 < K \ll 2 \tag{4.51}$$

and for all other values of K, Y_2 and Y_3 are inductors.

From equation (4.41) – (4.43), Y_2' and Y_3' are given by:

$$Y_2' = \sqrt{\frac{2}{K}}\ \cos\theta_1 - 1 \tag{4.52}$$

$$Y_3' = \sqrt{\frac{2}{K}}\ \cos\theta_1 - \frac{1}{K} \tag{4.53}$$

Odd mode chain matrix is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} \cos\theta_1 - Z_1' \sin\theta_1\,(Y_3' + 2Y_5') & jZ_1' \sin\theta_1 \\ j(Y_2' + 2Y_4')\cos\theta_1 + \frac{j}{Z_1'}\sin\theta_1 + j(Y_3' + 2Y_5')(\cos\theta_1 - (Y_2' + 2Y_4')Z_1' \sin\theta_1) & \cos\theta_1 - Y_2'Z_1' \sin\theta_1 \end{bmatrix} \tag{4.54}$$

From equation (4.30) – (4.31), (4.40) – (4.43) and (4.48), Y_4' and Y_5' are given by:

$$Y_4' = 1 \tag{4.55}$$

$$Y_5' = \frac{1}{K} \tag{4.56}$$

Hence the design steps of proposed impedance transforming inductor less quadrature hybrid can be summarized as:

Step1: Selection of θ_1 and Z_1 from:

$$Z_1 \sin\theta_1 = Z_0\sqrt{\frac{K}{2}} \tag{4.57}$$

where $\theta_1 > \cos^{-1}\left(\frac{1}{\sqrt{2K}}\right)$ for $0.5 \ll K \ll 1$ and $\theta_1 > \cos^{-1}\left(\sqrt{\frac{K}{2}}\right)$ for $1 < K \ll 2$. θ_1 and Z_1 should be chosen such that a realizable and miniaturized through line of hybrid can be implemented.

Step2: Computation of other element values from following design equation based on chosen θ_1 and Z_1.

$$Y_2 = \frac{1}{Z_0}\left(\sqrt{\frac{2}{K}}\cos\theta_1 - 1\right) \tag{4.58}$$

$$Y_3 = \frac{1}{Z_0}\left(\sqrt{\frac{2}{K}}\cos\theta_1 - \frac{1}{K}\right) \tag{4.59}$$

$$Y_4 = \frac{1}{Z_0} \tag{4.60}$$

$$Y_5 = \frac{1}{KZ_0} \tag{4.61}$$

Fig. 4-20 shows the through port and coupled port response of proposed

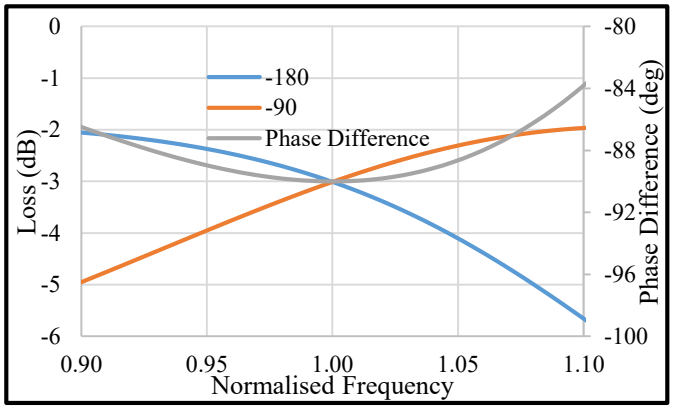


Figure 4-20. Insertion and coupled path response of proposed hybrid.

impedance transforming quasi-lumped element hybrid. The proposed hybrid had amplitude imbalance and phase imbalance of better than 1dB and 2^0 over 10% of fractional bandwidth. Further improvement in operational bandwidth of the hybrid can be achieved using multi-section topology with each section designed using the above mentioned design equations.

4.3 Design and Simulation of 200W MMIC High Power Impedance Transforming Quasi-Lumped Element Hybrid at S-band

For realizing 200W GaN T/R Switch, as explained in 3.2.3, the input quadrature hybrid needs to be an impedance transforming, MMIC based, high power and low loss quadrature hybrid. The "modified" lumped element quadrature hybrid proposed in 4.2.5 is employed. An impedance transforming quadrature hybrid at input and output is used to transform the impedance from Z_0 to lower impedance and lower impedance to Z_0 respectively. Fig. 4.21 shows the schematic of an S-Band impedance transforming quasi-lumped element quadrature hybrid.

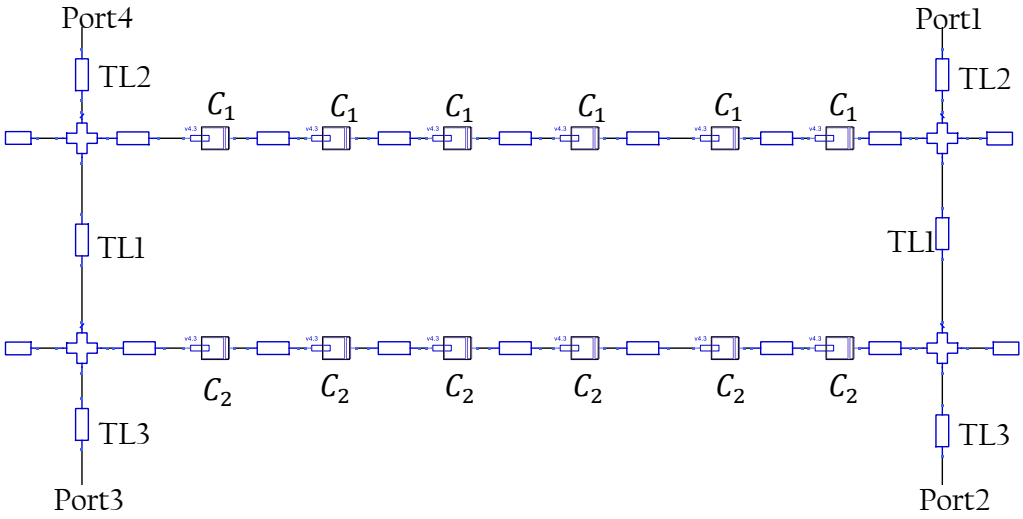


Figure 4-21. Schematic of proposed impedance transforming hybrid at S-Band using GH25 process of UMS foundry

The circuit is designed using 250nm GaN process, GH25, of UMS foundry with 50 Ω input impedance and 25 Ω output impedance. The current handling capability of top metal layer in GH25 process is 47mA/μm and breakdown voltage of metal-insulator-metal (MIM) capacitor is 35V. To increase the power handling capability of the hybrid, selection of series arm electrical length is done such that the hybrid is

inductor less. The series arm of the hybrid with impedance, Z_1 is realized using transmission line, TL1 with electrical length, θ_1 = 320. It can be shown using equation (4.57) that with the chosen value of K and θ_1 the shunt element will be capacitive. Using equation (4.57), Z_1 = 47Ω. The physical length of the line, TL1, for 320° electrical length is 2.88mm for hybrid operating at 3200±40 MHz.

As the physical length of TL1 is very large, it is wiggled to realize the hybrid in a compact size. The shunt arm admittance, Y_4 and Y_5, is derived from equation (4.60) – (4.61) and is equal to 0.02 Ω and 0.04 Ω respectively. These shunt arm admittance of the hybrid, Y_4 and Y_5, is realized using metal-insulator-metal (MIM) capacitor C_1 and C_2. Five numbers of series capacitor are placed in each shunt arm to limit the voltage swing across the capacitor, to less than the rated 35V, when 200W power is fed to the input port of the hybrid. Five numbers of 6pF capacitor are connected in series to realize the required admittance Y_4 whereas five numbers of 12pF capacitor is connected in series to realize the required admittance Y_5. Short stub admittance, Y_2 and Y_3 are derived from equation (4.58) – (4.59) and is equal to 0.01 Ω and ~ 0 Ω. Short stubs with admittance Y_2 and Y_3 is realized using open stubs TL2 and TL3 respectively. As Y_3 admittance is approximately short, TL3 may be omitted from the design without affecting the performance of the hybrid.

Schematic simulation is carried out using ADS software to evaluate the performance of hybrid and fine tune its element value. As mentioned previously, TL1 and TL2 lines are wiggled to shrink the size of the layout. As the admittance of TL3 is very large, they are omitted from the layout without effecting the electrical performance of the hybrid. An electromagnetic simulation was done to extract the parasitic and was

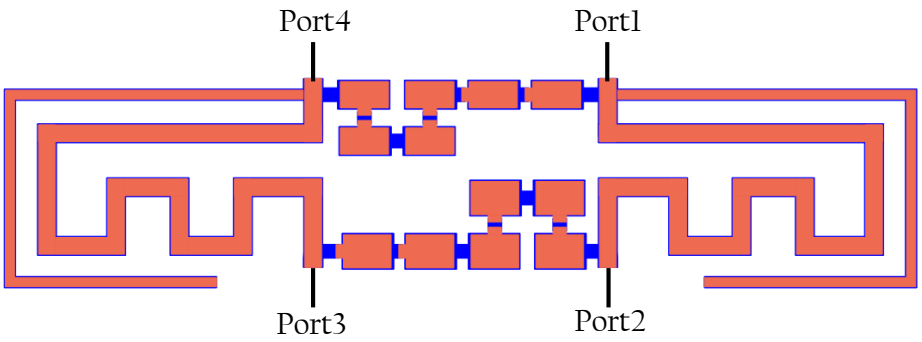


Figure 4-22. Layout of proposed impedance transforming hybrid at S-Band using GH25 process of UMS foundry

then subsequently compensated by tuning the component values of the hybrid. Fig. 4.22 shows the layout of the hybrid.

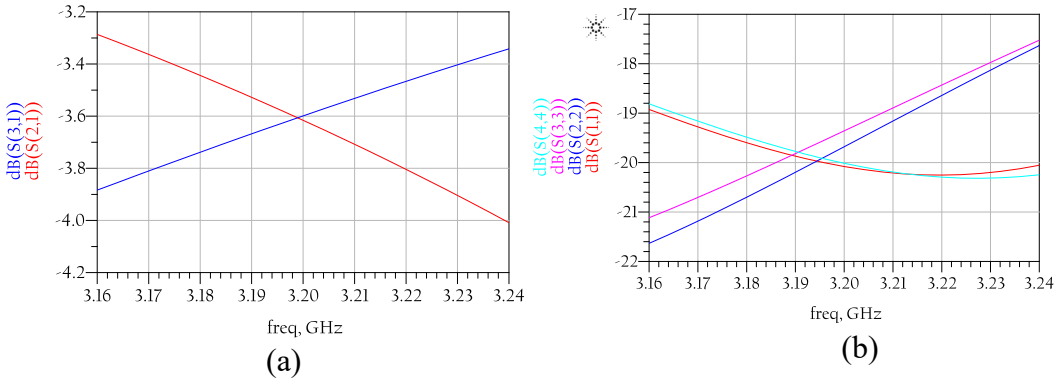


Figure 4-24. Simulated insertion loss and return loss of proposed quadrature hybrid (a): Insertion Loss. (b): Return Loss

Fig. 4-23 and Fig. 4-24 shows the EM simulation result of the hybrid at 3200±40 MHz. The simulated result follows closely to the proposed formulae of the hybrid. Insertion loss of 0.5 dB is due to the conductor loss of transmission line in series arm. Amplitude and phase balance of hybrid is less than 0.6dB and 40 respectively. Return loss at all the ports of hybrid is better than 17dB, whereas isolation is better than 18dB

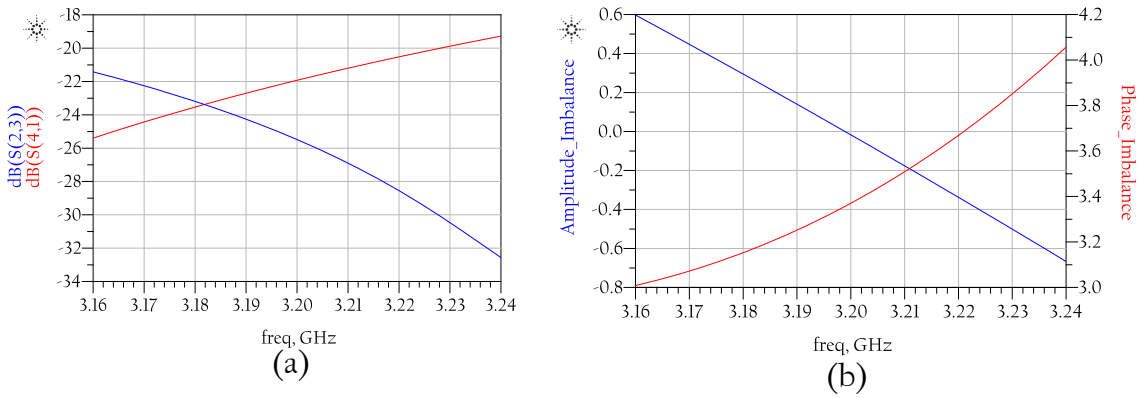


Figure 4-23. Simulated isolation and imbalance of proposed quadrature hybrid (a) Isolation. (b) Amplitude and Phase Imbalance

across the desired bandwidth. Table 4.1 shows the summary of the values of the components used in designing the hybrid.

TABLE 4.1:
Component Values of Proposed Hybrid

Component Name	Component Value
TL1	$Z_1 = 47\Omega$, $\theta_1 = 32^0$
Y_2	0.014 Ω

Y_3	~0 Ω
Y_4	0.02 Ω
Y_5	0.04 Ω

4.4 Design and Simulation of 20W MMIC High Power Compact Wideband Spiral Hybrid (D01PHS process of M/s OMMIC)

For realizing 20W GaAs T/R Switch, as explained in 3.2.4.1, the input quadrature hybrid needs to be MMIC based, compact, high power and low loss quadrature hybrid. As the GaAs real estate, i.e MMIC chip area, is at a premium, and two hybrids are needed, one each at input and output, for realizing a high power switch, the hybrid has to be compact. Hence the compact spiral quadrature hybrid is chosen as the required configuration.

Figure 4.25 shows the schematic of the compact spiral quadrature hybrid, as explained in section 4.2.3.

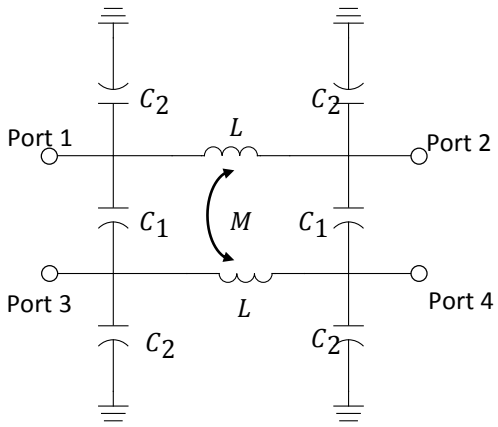


Figure 4.25. Schematic of equivalent circuit of compact wide-band spiral quadrature hybrid

The hybrid is designed at 9600±300 MHz with 20 W input power handling capability using 130nm process, D01PHS, of OMMIC foundry. Using equation (4.30) - (4.33), lumped elements of its equivalent circuit are calculated. Series arm inductor, L is equal to 1.17nH whereas mutual inductance between series arm inductor is calculated as 0.83nH. The shunt capacitors of the hybrid, C1, C2, is evaluated as 3pF and 1.25pF respectively. The schematic simulation of the equivalent circuit is performed using ADS and the simulation results confirm to the derived equations (4.22) – (4.25) for 3dB quadrature hybrid.

As the required power handling capability is 20W, the width of the transmission line, required to realize multi-turn inductor, is chosen such that maximum current flow is below the rated value. The maximum current density in the top metal layer of D01PHS process is 12mA/μm. Mutual inductance between the sandwiched inductors is controlled by the gap between the inductor turns. Due to narrow gap, intense electric field is generated when input power to hybrid is high. The maximum allowed potential difference between two adjacent top metal in 20 V for the selected process. Hence, the width of transmission line of inductors and its gap is selected such that current density and potential difference between the adjacent line is less than 12mA/μm and 20V respectively. A trade-off is made between the larger width/gap of the transmission line and size of the hybrid.

Fig. 4-26 shows the layout of compact wideband spiral quadrature hybrid at X-Band.

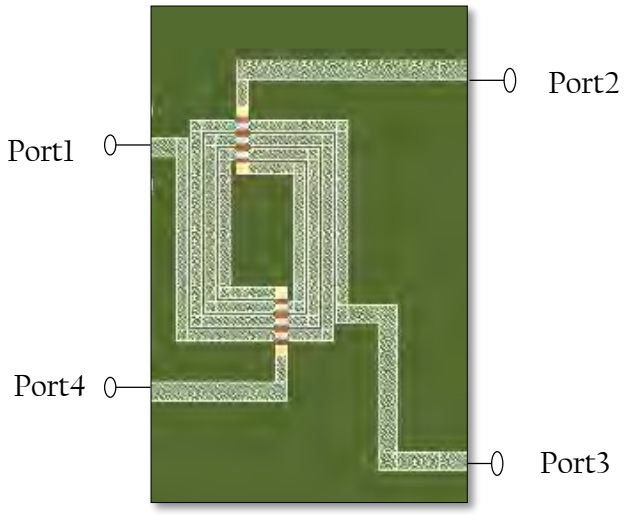


Fig. 4-26. Layout of proposed compact spiral hybrid at X-Band using D01PHS process of OMMIC foundry

As discussed in 4.2.3, series arm inductor is realized using transmission line and mutual coupling between inductor is realized by sandwiching the two inductor with inner and outer spiral windings. Width of the transmission line governs the width of the air-bridge for cross over. It is selected judiciously such that it is wide enough to handle 20 W of power and the hybrid is also compact in size. Using equation (4.30) and equation (4.33), the length of the line and gap between the inner and outer spiral

winding is calculated at 9600±300 MHz.

Electromagnetic simulation of the layout is performed using ADS to extract the parasitic and the effect of air bridge which is required for connection of two output ports to the internal windings. Compensation of parasitic and air-bridge is done in co-simulation to achieve the desired results. Figure 4.27 and figure 4.28 shows the simulated result of proposed compact spiral quadrature hybrid. Insertion loss is better than 0.6 dB and return loss at all the ports of the hybrid is better than 15dB. The proposed hybrid demonstrates an excellent isolation of better than 22dB across the desired bandwidth and amplitude and phase imbalance of better than 0.4 dB and 4^0 respectively.

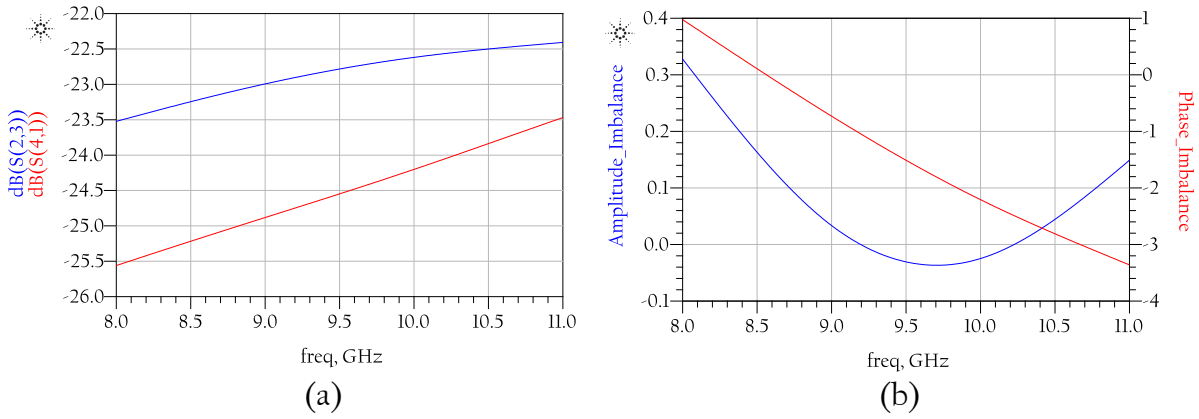


Figure 4.27. Simulated isolation and imbalance of proposed quadrature hybrid (a) Isolation. (b) Amplitude and Phase Imbalance

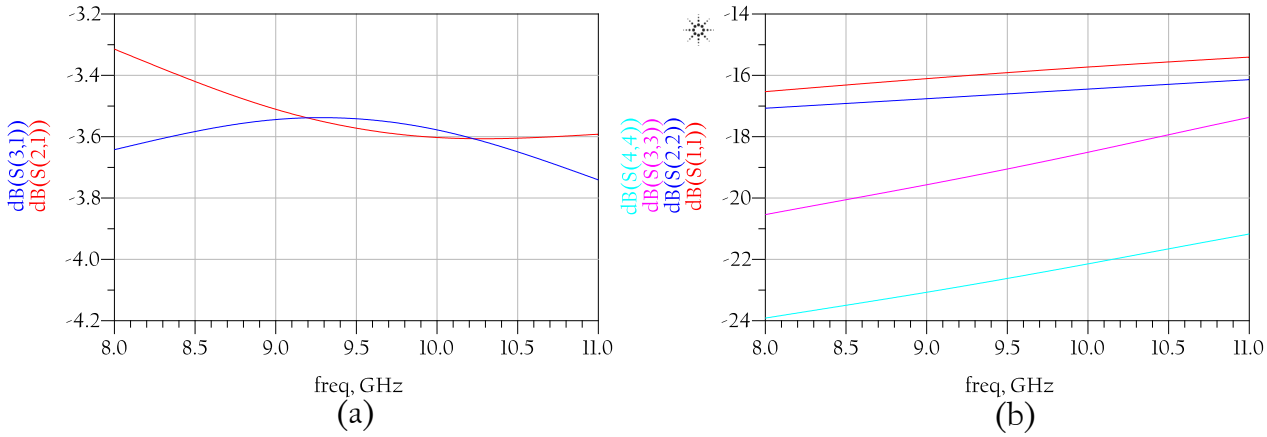


Figure 4.28. Simulated insertion loss and return loss of proposed spiral hybrid (a) Insertion Loss. (b) Return Loss

4.5 Design and Simulation of 10W MMIC High Power Compact Wideband Spiral Hybrid (PH25 process of M/s UMS)

For realizing 10W GaAs T/R Switch, as explained in 3.2.2.1, the input quadrature hybrid needs to be MMIC based, compact, high power and low loss quadrature hybrid. As the GaAs real estate, i.e MMIC chip area, is at a premium, and two hybrids are needed, one each at input and output, for realizing a high power switch, the hybrid has to be compact.

Conventional, branch line coupler was the first choice but the size was not suitable even after meandering considering the MMIC realization. Lange coupler was the next option but not suitable considering the involved line widths (6 + 6 μm) for power handling. The process allowed a maximum of I_{rms} of 47 mA/μm for main metallization layer and 22 mA/μm for underpass metallization. The RMS current in input line for 10W was 632 *0.707(rms factor) * 1.414 (derating factor) = 632 mA requiring a line width of at least 14 μm, thereby making it unsuitable for even 10W.

Hence the compact spiral quadrature hybrid, as was used in section 4.4, is chosen as the required configuration. The hybrid is designed at 9600±300 MHz with >10 W input power handling capability using 250nm process, PH25, of UMS foundry. Using equation (4.30) - (4.33), lumped elements of its equivalent circuit are calculated. The schematic simulation of the equivalent circuit is performed using ADS and the simulation results confirm to the derived equations for 3dB quadrature hybrid. As the required power handling capability is >10W, the width of the transmission line, required to realize multi-turn inductor, is chosen such that maximum current flow is below the rated value. The power handling in this hybrid is limited by underpass width, which being 49 μm can carry maximum of 49 * 22 =1078 mA de-rated RF current. This current corresponds to an input RF power of 41.6 dBm when the hybrid and switch are lossless. Therefore, this hybrid can handle input de-rated power of > 14W and is suitable for this MMIC application. Figure 4.29 shows the layout of compact wideband spiral quadrature hybrid at X-Band

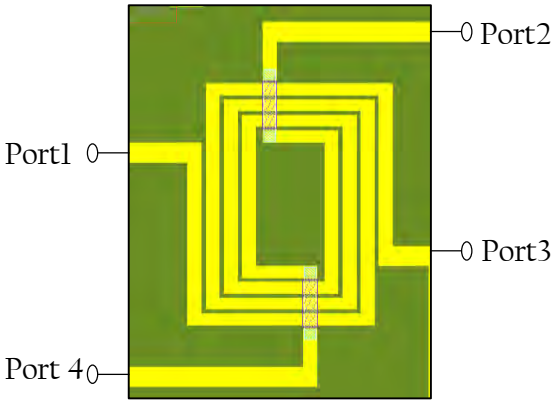
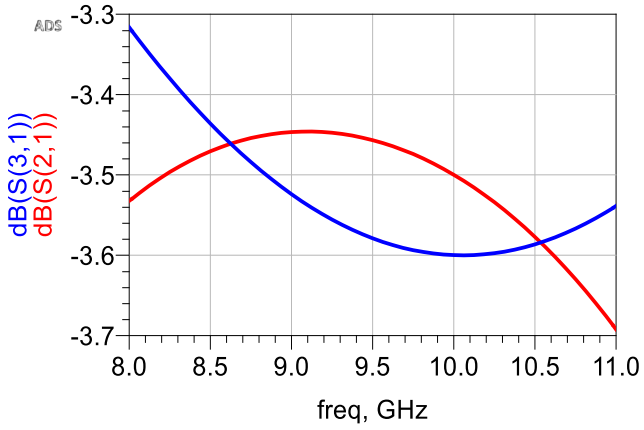


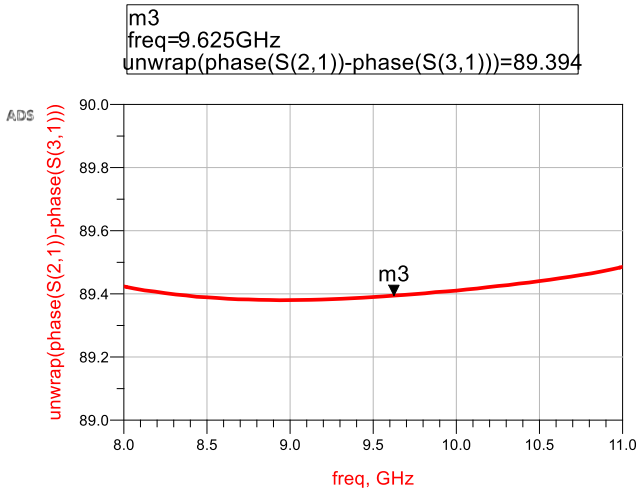
Figure 4.29. Layout of proposed compact spiral hybrid at X-Band using PH25 process of UMS foundry

As discussed in 4.2.3, series arm inductor is realized using transmission line and mutual coupling between inductor is realized by sandwiching the two inductor with inner and outer spiral windings. Width of the transmission line governs the width of the air-bridge for cross over. It is selected judiciously such that it is wide enough to handle 10 W of power and the hybrid is also compact in size. Using equation (4.30) and equation (4.33), the length of the line and gap between the inner and outer spiral winding is calculated at 9600±300 MHz.

Electromagnetic simulation of the layout is performed using ADS to extract the parasitic and the effect of air bridge, which is required for connection of two output ports to the internal windings. Compensation of parasitic and air-bridge is done in co-simulation to achieve the desired results. Figure 4.30 and figure 4.31 shows the simulated result of the proposed compact spiral quadrature hybrid. Insertion loss is better than 0.6 dB and return loss at all the ports of the hybrid is better than 15dB across the band.



(a)



(b)

Figure 4.30. Simulated results of 10W quadrature hybrid (a) Insertion Losses and (b) Phase Imbalance

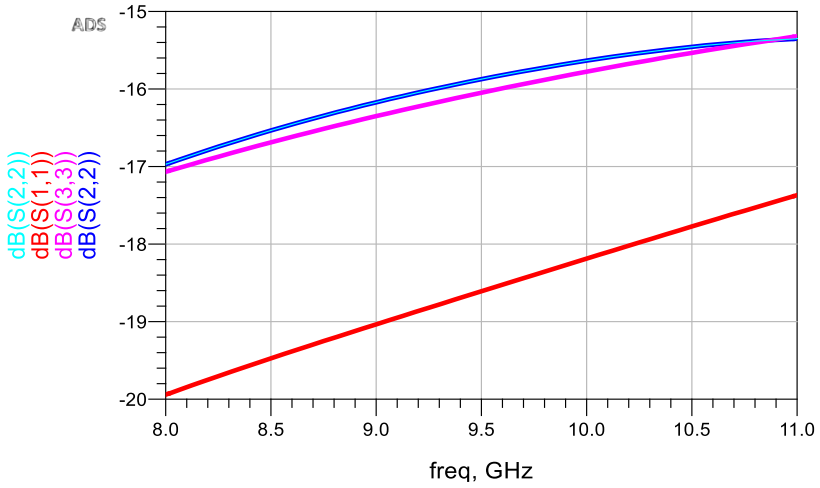


Figure 4.31. Simulated return loss of proposed spiral hybrid

4.6 Conclusions

- Employing the proposed modified lumped element impedance transforming quadrature hybrid, compact 200W, 50Ω to 25Ω impedance transforming quadrature hybrid over 3200 ± 40 MHz has been designed and simulated. Simulation results show amplitude and phase balances of less than 0.6 dB and 4° respectively. Return loss at all the ports of hybrid is better than 17dB whereas isolation is > 18dB across the desired bandwidth, designed using 0.25 µm GaN process (GH25 of M/s UMS).

- The 20W quadrature hybrid is designed using 0.13 µm GaAs process (D01PHS of

M/s OMMIC), employing compact spiral hybrid architecture. The simulation results show insertion loss better than 0.6 dB and return loss at all the ports of the hybrid better than 15dB. The proposed hybrid demonstrates an excellent isolation of better than 22dB across the desired bandwidth and amplitude and phase imbalance of better than 0.4 dB and 4^0 respectively.

- The 10W quadrature hybrid is designed using 0.25 µm GaAs process (PH25 of M/s OMMIC), employing compact spiral hybrid architecture. The simulation results show insertion loss better than 0.6 dB with less than ±0.1 dB amplitude imbalance and less than 1° phase imbalance with return loss at all the ports of the hybrid better than 15dB across the band.

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Chapter: 5

MMIC Switches

5.0 Introduction

Switches are classified based on their number of poles and throws, where pole refers to number of individual circuits that can be switched while throw refers to possible connection of the individual circuit. Mostly used switch types are listed below:

(a) Single Pole Single Throw (SPST) switch

(b) Single-Pole Double-Throw (SPDT) switch

(c) Double-Pole Single-Throw (DPST) switch

(d) Double-Pole Double-Throw (DPDT) switch

SPST switch has one input terminal which connects to one output terminal. SPDT switch has one input which can be connected to two outputs. DPST switches have two input and two output terminals which could be connected to provide a single RF path out of the two input chains. DPDT switches are more complex than other switches and are mostly used in radar systems having two inputs that could be connected to either of the two outputs. Fig. 5.1 shows the typical signal flow for the above mentioned switches.

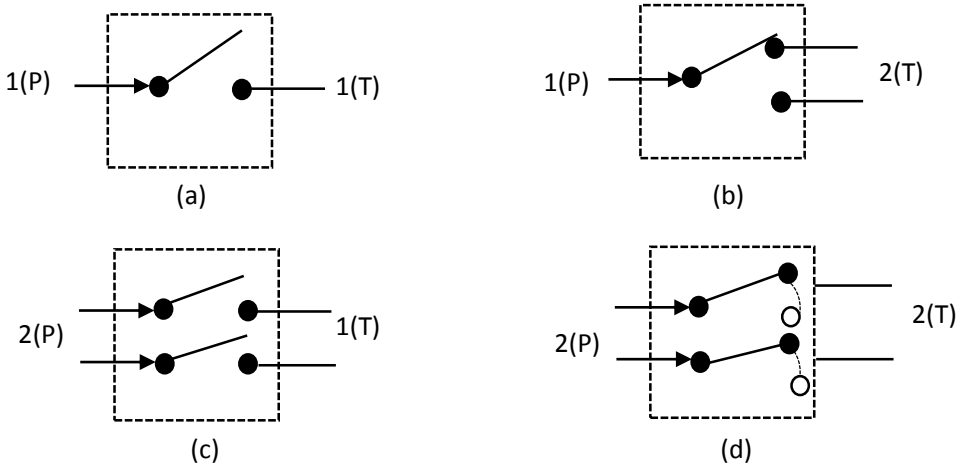

Figure 5-1. Switch Configuration (a): SPST (b): SPDT (c): DPST (d): DPDT

The switches can further be classified in either absorptive or reflective configuration. Reflective switch as the name indicates, when the port which is not connected or it is open and any signal present at this port will be reflected. The reflective switch is easier to design and provides less insertion loss [1]. In the absorptive configuration, the incident signal at the port which is not connected is not reflected back

but absorbed in a termination whose resistance is exactly equal to the characteristic impedance, Z_0, of the transmission line. In radar applications for design of protection switch / T/R switch, the absorptive configuration is preferred, to avoid generation of standing waves. In the insertion loss state, the termination is disconnected from the transmission line, thereby allowing all of the incident energy to propagate through the switch. Fig. 5-2 below shows the absorptive SPST switch configuration where Z_O resistance is realized by a series combination of FET and series resistance.

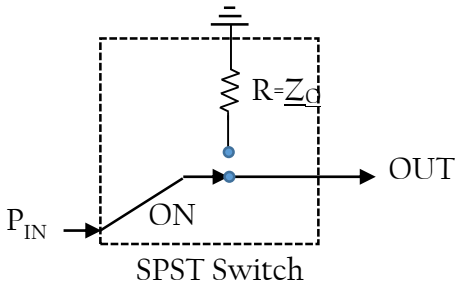

Figure 5-2. Absorptive SPST Switch Configuration

5.1 Design and implementation of conventional MMIC Switches

It is important to characterize the switch performance by specifying basic design parameters. An ideal switch (T/R switch or protection switch) is defined by:

- **Insertion Loss (IL):** It is expressed as a ratio of the power delivered to the load in ON state of the ideal switch to the ideal power delivered by the practical switch in ON state. Low insertion loss is desirable to minimize the receiver noise figure and maximize the transmitted power to the antenna.
- **Isolation:** It is expressed as a ratio of the power delivered to the load in ON state to the power delivered to the load in the OFF state. High isolation is desirable to protect the sensitive receiver circuitry from transmit signal leakage.
- **Power Handling capability:** It is an essential requirement for the switch to be used in high power applications without being damaged.
- **Switching time:** Fast switching time is essential to reduce radar blind times.
- Small physical size and suitable for monolithic integration
- **Power consumption**: Simple bias/control requirements to reduce design complexity and power consumption.

The primary devices used for the switches could be PIN diodes, GaAs MESFET and p-HEMT, Si MOSFET, SiGe HBTs and GaN HEMTs [1]. Both diodes based and

transistor based switches are commonly used for various applications. PIN diodes and transistor based technologies are compared in this section.

PIN diodes are current controlled device having high resistivity intrinsic (I) region sandwiched between p-type and n-type semiconductor The PIN diodes are used as switching element, to present either a short circuit or an open circuit, depending on the bias condition viz. its reverse and forward bias characteristics. The performance characteristics of the PIN diode depends mainly on the chip geometry and the processed semiconductor material in the intrinsic or I - region. It determines the switching speed, capacitance, breakdown voltage etc. [1]. PIN diodes can be fabricated on Si and GaAs substrate and the main benefit of PIN diode is that it can handle large RF signals. The flip side characteristics of PIN diode based switches are complex bias requirement, finite reverse recovery time, and non-compatibility of monolithic integration.

In switch design based on FET, which acts as voltage-controlled resistor, source and drain ports form a channel while gate act as control terminal. Fig. 5-3 shows the simplified cross-section of a conventional FET structure.

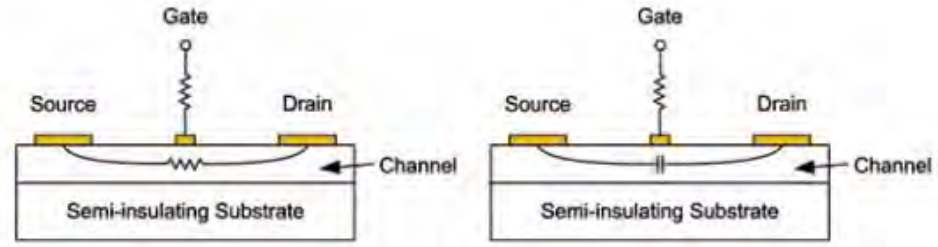

Figure 5-3. Simplified FET circuit ON and OFF path [13]

In reverse bias, C_{off} is a combination of depletion layer capacitance and source drain capacitance while R_{off} is a function of frequency and leakage resistance [2]. In depletion mode FET configuration, the channel is normally in its low impedance state with no control voltage applied. When a negative gate-source voltage is applied to an n-channel depletion type FET, the channel region is completely depleted of free charge carriers and is in high impedance, pinched off state. Under these conditions, the FET can be modelled by series and parallel combinations of resistors and capacitors as

(a) (b)

Figure 5-4. Simplified FET equivalent circuit
(a) forward and (b) reverse bias

shown in Fig. 5-4.

In most applications, the gate voltage is typically about 1.5 times the pinch-off voltage, however for high power application or GaN based switches, the control voltage is much higher than pinch-off voltage [1]. The inherent advantages of FET based switches over PIN diode switches is simplified bias network, small or negligible DC power requirement, simplified driver circuit, faster switching speed, monolithic implementation, ease of integrality with other functionality without the need of additional external components [1]. High Electron Mobility transistors (HEMT) are also used as basic control element in the same way as FET, only device structure is different [1]. Distinct advantages are low ON resistance and small OFF capacitance, which results in lower loss and good isolation characteristics at high frequencies [1]. GaN HEMT based devices, when compared to GaAs HEMT, have higher power handling capability, high breakdown voltage, and high thermal conductivity (GaN HEMT can be grown on SiC substrates), greatly helps the devices for high power density operation.

There are three basic configurations used for switch design: using FET either in series, shunt or combination of both. In the series configuration shown in Fig. 5.5(a), the FET is connected in series of a transmission path with one port connected to input while the other is connected to the output. During ON state, Q_1 is turned on and the signal flows from input to output (port P_{IN} to P_1), while during OFF state, Q_1 is turned off and the signal is attenuated. In shunt configuration shown in Fig. 5.5 (b) one port is connected to the transmission line while the other is grounded. In shunt configuration, FET has complementary function compared to series configuration viz. in on state, signal is terminated while in high impedance state, the signal appears at the output. In both the configuration, the signal is reflected back to the input (open or short) when

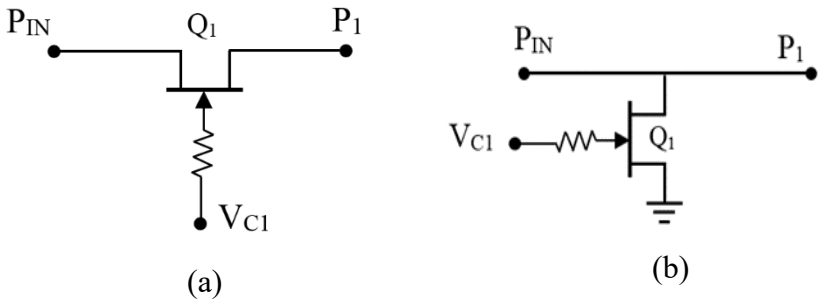

Figure 5-5. Simplified schematic of SPST switch
(a) series and (b) shunt configuration

signal is not transmitted to output.

Because of non-zero impedance of FET in ON state while non-infinite impedance in OFF state the switching functions are not flawless [2]. However, there is always a small fraction of power that is dissipated in series resistance during transmission or leaked to the output during isolation state. The figure of merit of a switch is defined in terms of insertion loss and isolation. Insertion loss (IL) is defined as a ratio of power delivered to load to actual input power, while isolation is defined as a ratio of output power that appears at the output in on and off state. In the ON-state, the low channel resistance of the FET is the major governing parameter and has nearly independent frequency response. In the OFF-state, however, the equivalent capacitance of the circuit dominates and displays frequency dependence. Therefore, IL for the series FET and isolation for the shunt FET configurations, both in the on-state, show frequency invariant performance. On the other hand, isolation for the series FET and IL for the shunt FET topology, both in the off-state, show frequency variant performance [1]. Due to above behavior, better performance is achieved if both the devices viz. series and shunt elements are connected together as shown in Fig. 5-6. The switch is ON when the series device is in low impedance state and shunt device in high impedance state by virtue of two control signals. Similarly, in OFF state of the switch, the series device is OFF and the shunt device is ON.

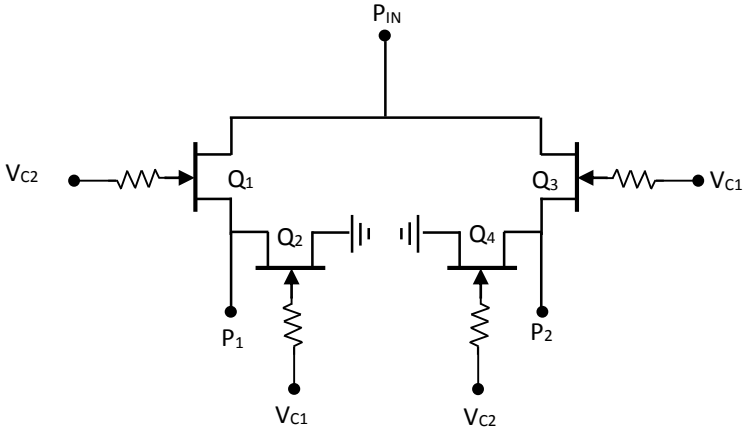

Figure 5-6. Simplified schematic of SPDT switch series shunt configuration

Isolation is better than both series/shunt only configuration switches, but it results in higher insertion loss than shunt switch. In series shunt configuration, the insertion loss of the "ON" path of the switch is affected by the "ON" channel resistance, which is determined by FET periphery. Likewise, the isolation of the "OFF" path is limited by

the capacitance created by the source and drain spacing as well as FET physical size (periphery). Increasing the FET size decreases its on-state resistance and thus reduces IL. However, it also results in larger gate-source and gate-drain capacitance and increased source-drain fringing capacitance, which restricts the switch performance in the off-state [1].

5.2 Design and Realization of 10W T/R switch (PH25 GaAs process of UMS)

Following the design approach presented in 3.2.2.1, in the present work, a shunt resonant HEMT switch enabled DPDT configuration is employed for realizing Transmit/Receive switch while employing the technique of on-the-chip coherent current distribution to design a 10W T/R switch. The design has been implemented on standard commercially accessible 0.25µm pHEMT low power, low noise process (PH25-UMS foundry).

5.2.1 High Power Switch Element

The low noise pHEMT process (PH25) is having typical parameters like V_p =-0.75V, V_{DS} max=7V, $I_{DSS\ typ.}$=350mA/mm, largest characterized gate periphery of 600 µm (8x75µm), Θj =150°C/W with $R_{DS\ ON}$= 4.0Ω and $R_{DS\ OFF}$ = 560Ω. For most of GaAs processes, the I_{DSS} variation across a wafer and across batches is as high as 30% and hence, the design has to be made for $I_{DSS\ typ.}$ rather than $I_{DSS\ max}$. For the chosen process, the $I_{DSS\ max}$ = 500 mA/mm and hence conservative $I_{DSS\ typ.}$ of 350mA/mm is used for design. *With $I_{DSS\ typ.}$ of 350mA/mm, the 600 µm gate periphery device can handle a $I_{DSS\text{-}pk}$ of 210mA.* As the device parameters used in the design viz., $I_{DSS\ typical}$, C_{DS}, R_{DS} are weak functions of temperature, the RF performance of T/R switch is not affected across a typical operating range of device of -15°C to 65°C. This process, in conventional configuration, yields a unit cell switch which has maximum power handling capability, Pmax, of 0.3W in low impedance state.

As can be seen from Fig. 3-9 and Fig. 3-10, a 300mW power handling capable FET device is employed to realize a 10W T/R Switch, with coherent current distribution across 4 identical devices, having transmit loss of 0.4 dB with receive isolation of 28 dB and receive loss of 1.4 dB. Fig. 5-7 shows the schematic of 10W high power TR switch designed using 250nm pseudomorphic HEMT process, PH25 of UMS foundry.

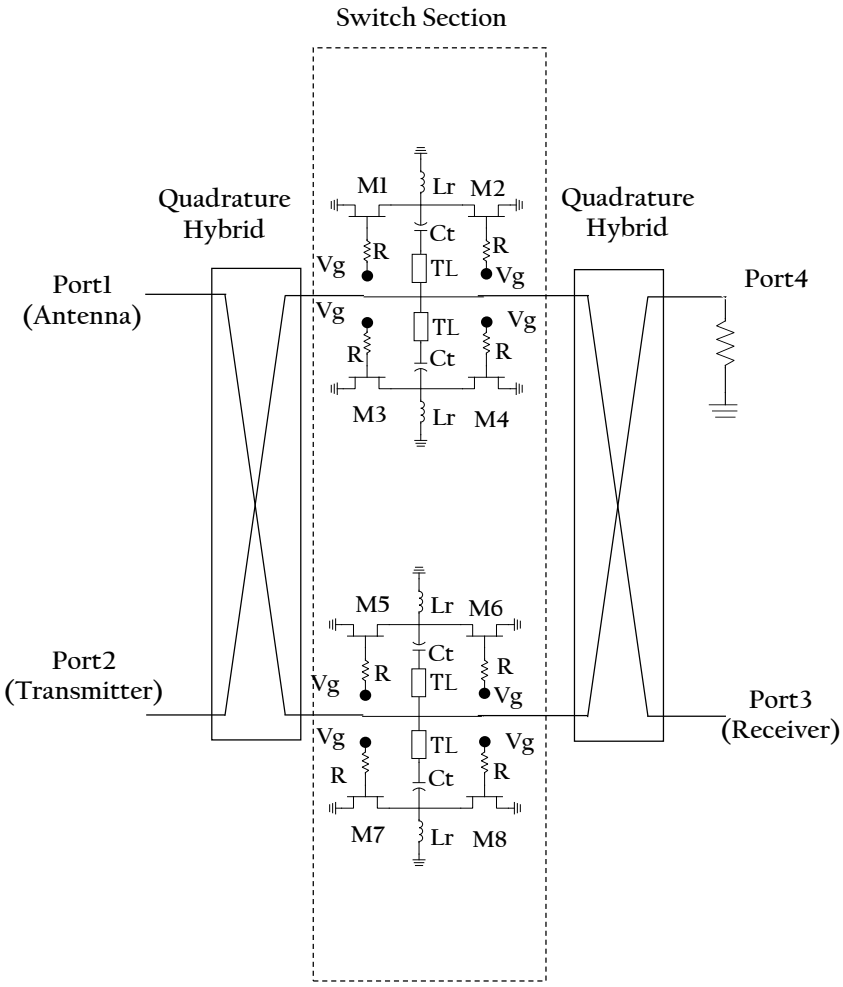

Figure 5-7. Schematic of 10W T/R Switch

The upper high power switch section is made up of M1 to M4 FETs connected in resonant shunt FET configuration. Exactly identical switch section made up of FETs M5 to M8 is used in the lower branch of the quadrature hybrid. During high power transmission, with gate control, Vg ≥ 0V, all the switching FETs viz., M1 to M4 and M5 to M8 are "ON", offering low shunt impedance, and so the high input power fed from Port2 is reflected from both the switches and gets added constructively at Port1 which is connected to Antenna, isolating the Receiver connected to Port 3.

While, during low power reception, with gate control, Vg ≤ pinch-off voltage, V_p, all the switching FETs viz., M1 to M4 and M5 to M8 are "OFF", offering large shunt impedance, and so power fed from Port 1 is constructively added at Port 3, isolating Port 2 and Port4, thus creating a T/R switch. In this switch architecture configuration, the individual switch sections need to handle only half the input power fed from Port1.

Table- 5-1

Component Values of 10W T/R Switch

Component	Value
Devices	8x75 µm gate width, 0.25 µm pHEMTs, 8 Nos.
L	0.42 nH
TL_I	125 µm
C_T	3 pF
Gate series Resistance, R_G	4000Ω

5.2.2 Input and Output Hybrids:

As shown in Fig. 5.7, both the switch sections are preceded and followed by a miniaturized 10W MMIC High Power Compact Wideband Spiral Hybrid (PH25 process of M/s UMS) designed and presented in section 4.2.3. The simulation results show insertion loss better than 0.6 dB with less than ±0.1 dB imbalance and less than 1° phase imbalance with return loss at all the ports of the hybrid better than 15dB across the band.

5.2.3 Layout and Simulation results

The input 3-dB quadrature hybrid, current paralleled SPST cells in each of the arms of the hybrid and the output 3-dB quadrature hybrid are integrated to create 10W T/R switch. The complete structure is simulated using harmonic balance analysis in CAD tool, Advanced Design System (ADS), with non-linear cold FET device model from the foundry. Fig. 5-8 shows the integrated 10W T/R Switch MMIC layout.

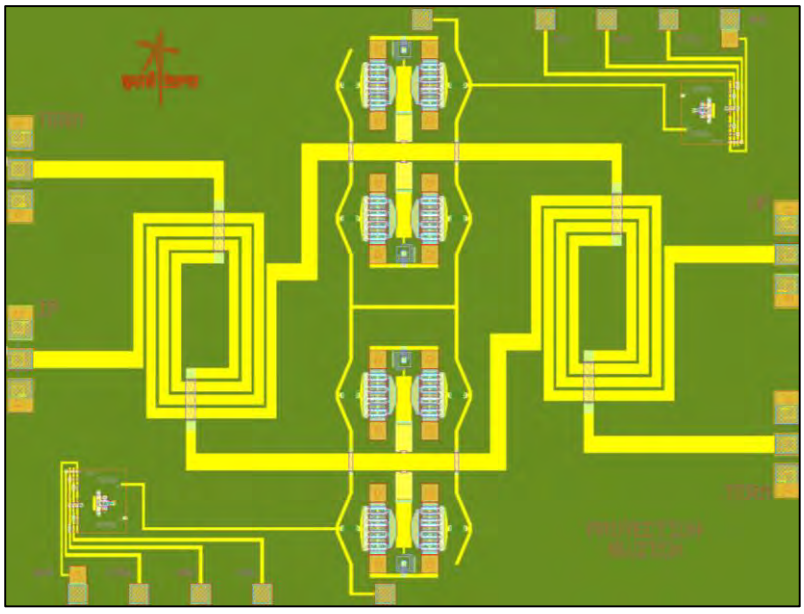

Figure 5-8. Layout of 10W high power T/R Switch

The dimensions of the 10W T/R switch MMIC are 3.9 x 2.8 mm. Fig. 5-9 shows the simulated coherent current distribution across 4 devices in one of the arms of the hybrid at 10W input at 9.6 GHz. It can be seen from Fig. 5-9, the current is distributed coherently across all the 4 devices within 10% spread and a maximum current of < 210mA, the limit of the device.

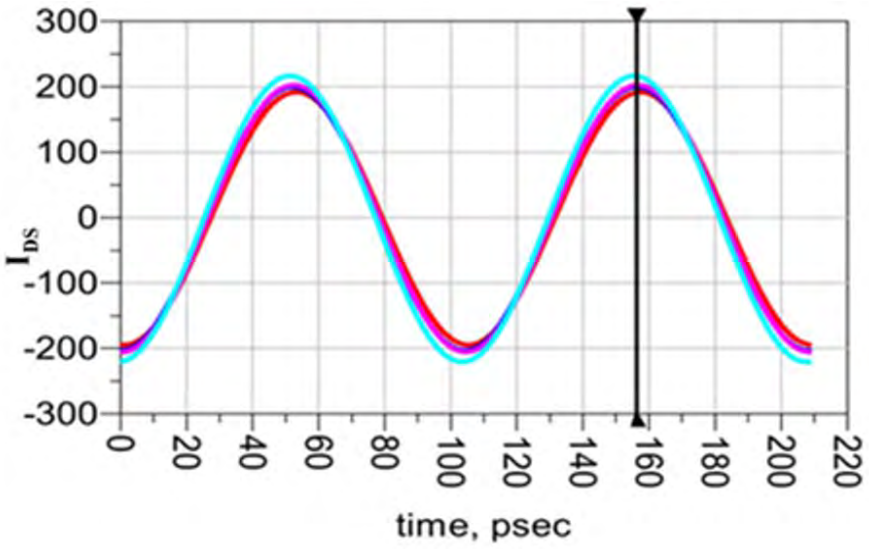

Figure 5-9. Current distribution across the FETs

5.2.4 Measurement results

Figure 5.10 shows the photograph of 10W T/R Switch under RF on-wafer testing. RF On-wafer testing has been carried for frequency response over 9.1-10 GHz for both transmit and receive mode conditions.

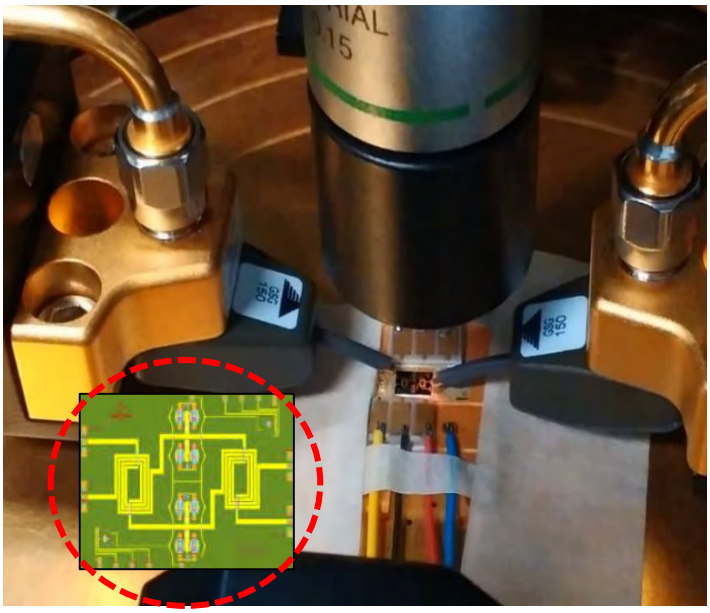

Figure 5-10. 10W T/R Switch under on-wafer testing with MMIC layout as inset.

Fig. 5.11 shows the comparison of simulated and on-wafer measured small signal transmit and receive path insertion losses along with input and output return losses. 5 MMICs across the wafer are on-wafer tested for high power performance of transmit path, under pulsed power condition (10% duty), to measure the power handling capability and the spread. Figure 5.12 shows the transmit path performance under power sweep conditions.

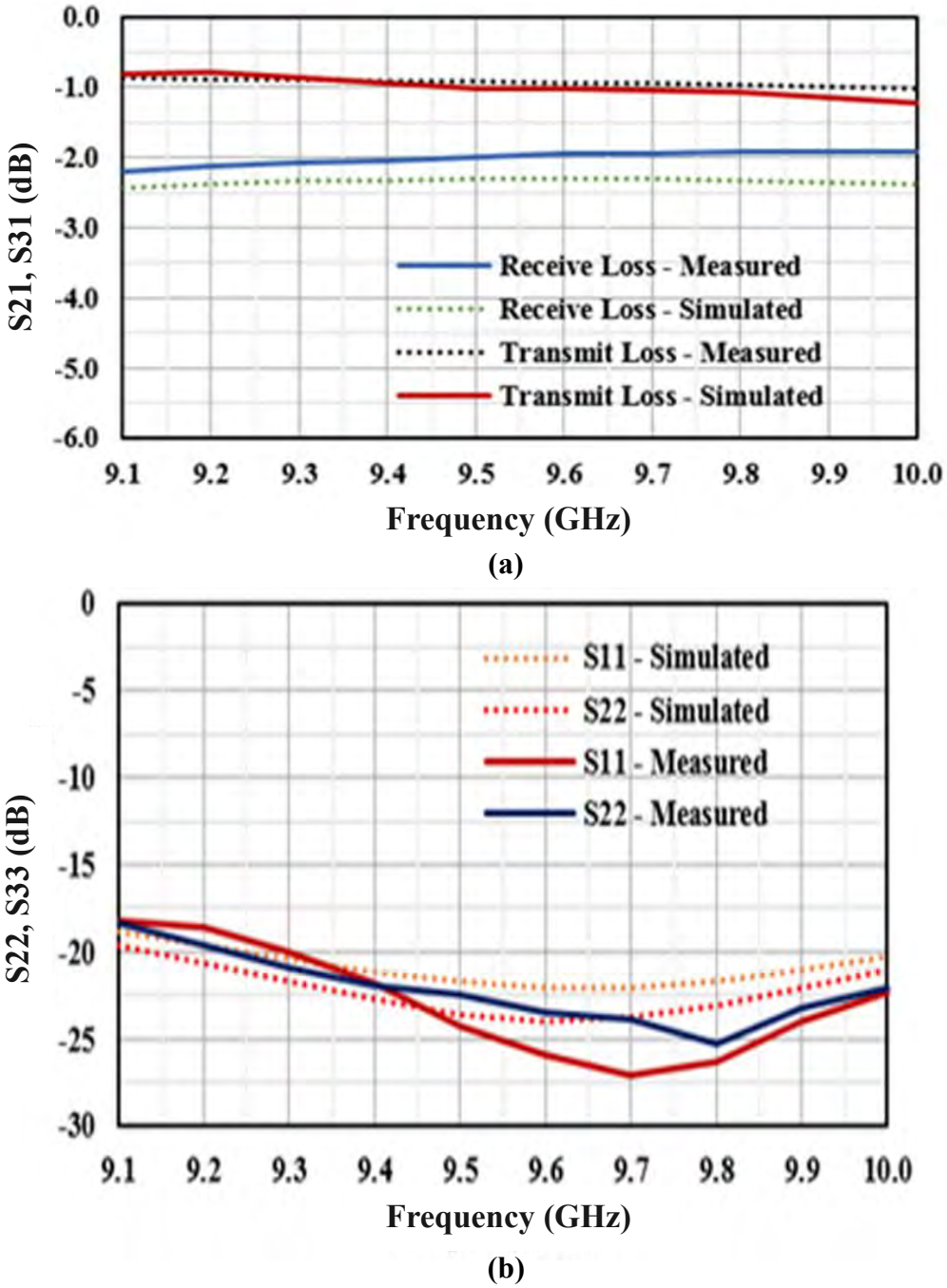

Figure 5-11. On-wafer High power T/R Switch small signal performance. (a): Transmit and receive path loss. (b): Return Losses

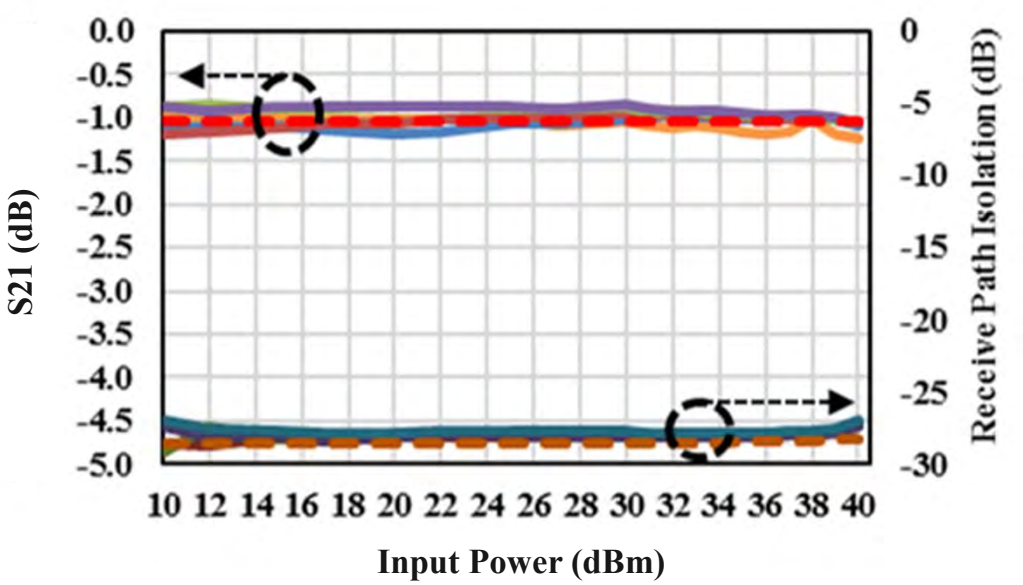

Figure 5-12. On-Wafer power sweep performance of high power T/R switch (Solid lines: measurement. Dashed lines: simulation)

Measured insertion loss varies from 0.95 dB to 1.2 dB against simulated value of 1.05 dB while the isolation varies around -27 to -28.5dB against the analyzed value of -28.3dB. Testing has been carried out up to only 10W (+40 dBm) because of setup constraints.

5.3 Design and Realization of 20W Receive Protection switch (D01PHS GaAs process of OMMIC)

The high power Receive Protection switch design is identical to Transmit/Receive Switch, however, unlike in the design of high power Transmit/Receive switch, in the design of Receiver protection switch, the insertion loss in the receive path is traded off with the insertion loss in the high power path.

5.3.1 High Power Switch Element

Following the design approach presented in 3.2.4.1, in the present work, a shunt resonant HEMT stacked switch enabled DPDT configuration is employed for realizing the Receive protection switch while employing the technique of *FET stacking along with on-the-chip coherent current distribution* to design a 20W switch. The design has been implemented on standard commercially accessible 0.13µm pHEMT low power, low noise process (D01PHS-OMMIC foundry).

The chosen, OMMIC-D01PHS low noise process has typical parameters like Vp=-0.9V, V_{DS} max=8V, $I_{DSS\ typ.}$=500mA/mm. The largest characterized gate periphery offered by the process is 600 µm (8x75µm), whose R_{DSON} and $R_{DS\ OFF}$ are 2.0 and 600Ω respectively. This process, in conventional configuration, yields a unit cell switch which has maximum power handling capability, Pmax, of 0.6W in low impedance state. As can be seen from Fig. 3-18 and Fig. 3-19, this 600mW power handling capable FET device is employed to realize a 20W T/R Switch, with coherent current distribution across 4 identical devices, having transmit loss of 0.17 dB with receive isolation of 34 dB and receive loss of 1.34 dB. Receive path loss can be reduced by reducing the no. of FETs paralleled but the power handling capability reduces significantly. Hence another novel technique viz., *FET Stacking with On-the-chip coherent Current distribution*, is proposed to improve Receive path loss without affecting the power handling capability of the T/R switch.

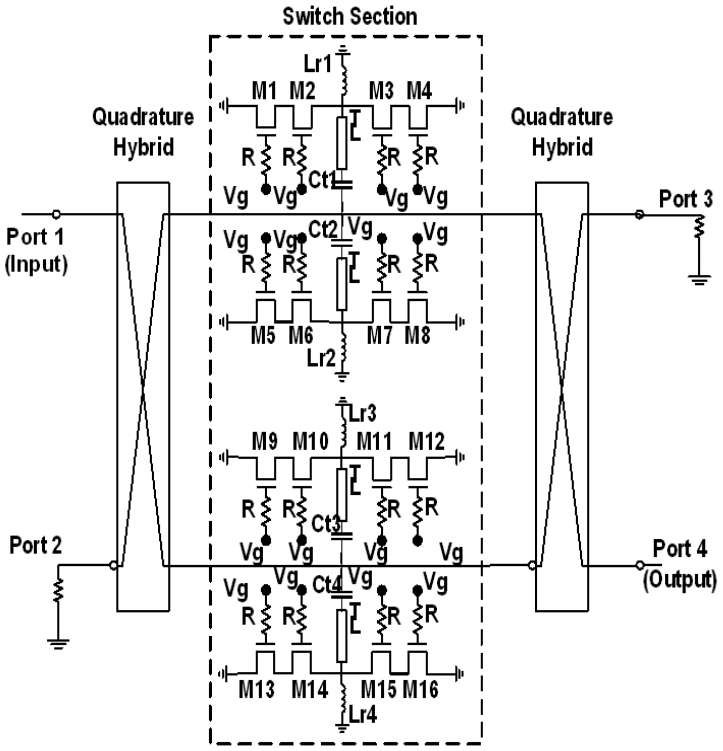

Figure 5-13. Schematic of 20W Receive Protection Switch

Figure 5.13 shows the schematic of the 20W high power TR switch designed using 130nm pseudomorphic HEMT process, D01PHS of OMMIC foundry. The upper high power switch section is made up of M1 to M8 FETs connected in *resonant shunt stacked FET configuration*. In resonant FET configuration, a shunt inductor, Lr,

connected across drain and source terminals is used to parallel resonate the drain-source capacitance, C_{DS}. Exactly identical switch section made up of FETs M9 to M16 is used in the lower branch of the quadrature hybrid. During high power transmission, with gate control, Vg ≥ 0V, all the switching FETs viz., M1 to M8 and M9 to M16 are "ON", offering low shunt impedance, and so the high input power fed from Port1 is reflected from both the switches and gets added constructively at Port2. Port 2 is connected to an off-chip high power termination, thus creating an absorptive protection switch. While, during low power reception, with gate control, Vg ≤ pinch-off voltage, Vp, all the switching FETs viz., M1 to M8 and M9 to M16 are "OFF", offering large shunt impedance, and so power fed from Port 1 is routed to the input of both LNAs.

TABLE 5-2
Component values of 20W switch

Component Name	Component Value
M1 to M16	8x75 µm gate width, 0.25 µm pHEMTs, 16 Nos.
Lr1, Lr2, Lr3, Lr4	0.68 nH
Ct1, Ct2, Ct3, Ct4	2.3 pF
R	4 kΩ
TL	50Ω, 22^0

5.3.2 Input and Output Hybrids:

As shown in Fig. 5.13, both the switch sections are preceded and followed by a miniaturized 20W MMIC High Power Compact Wideband Spiral Hybrid (D01PHS process of M/s OMMIC) designed and presented in section 4.2.3. The 20W quadrature hybrid is designed using 0.13 µm GaAs process (D01PHS of M/s OMMIC), employing compact spiral hybrid architecture. The simulation results show the insertion loss better than 0.6 dB and return loss at all the ports of the hybrid better than 15dB. The proposed hybrid demonstrates an excellent isolation of better than 22dB across the desired bandwidth and amplitude and phase imbalance of better than 0.4 dB and 4^0 respectively.

5.3.3 Switch Layout & Photograph

The input 3-dB quadrature hybrid, current paralleled SPST cells in each of the arms of the hybrid and the output 3-dB quadrature hybrid are integrated to create 20W Receive protection switch. The complete structure is simulated using harmonic balance analysis in CAD tool, Advanced Design System (ADS), with non-linear cold FET device model from the foundry. Fig. 5-14 shows the integrated 20W Receive Protection Switch MMIC layout and Fig. 5-15 shows the assembled MMIC. The dimensions of

the of 20W switch MMIC are 3.9 x 2.8 mm.

5.3.4 Measurement results

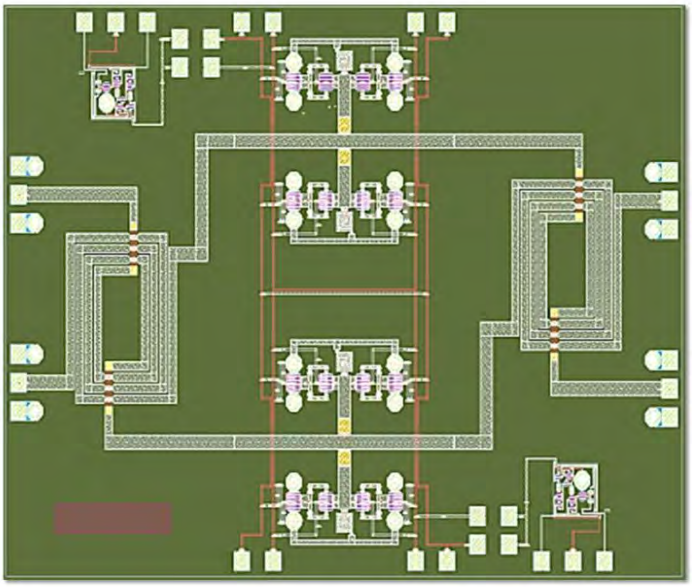

Figure 5-14. Layout of 20W Receive Protection Switch

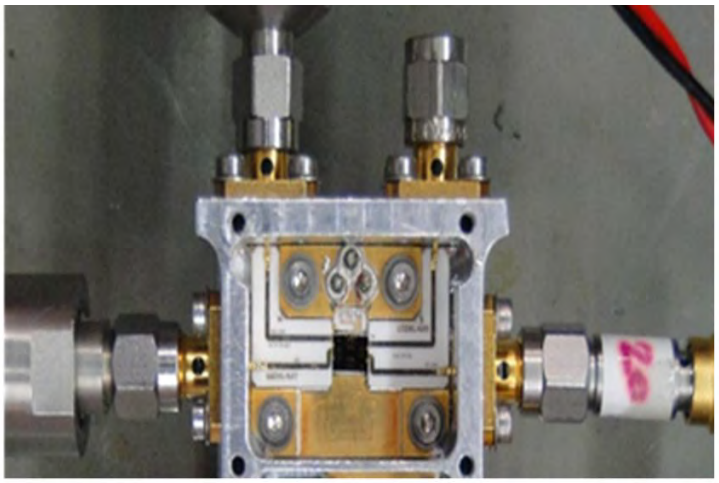

Figure 5-15. Assembled 20 W Receive Protection switch fabricated using D01PHS process of OMMIC foundry

For the 20W receive protection switch, the RF On-wafer performance testing has been carried out over 9.2-10 GHz for both transmit and receive mode conditions. Fig. 5.16 shows receive path insertion losses along with input and output return losses. The measured results of the 20W Receive protection switch MMIC is 2.3 dB insertion loss for the receive path. To test the 20W receive protection switch for power handling capability, the MMIC is mounted on a carrier plate and assembled in a test box with coaxial connectors on all the 4 ports, as shown in Figure 5.15. The switch is operated in transmit mode, i.e V_{GS}=0.5V. The input power to the switch has been varied and the output powers at transmit and receive ports have been measured on RF power meters.

The interconnect loss contribution of input and output connectors, link alumina substrates and interconnect bond wires is around 0.3 dB and is compensated in the presented results given in Figure 5-16. The transmit path insertion loss of 2.0 dB and the receive isolation of 28 dB remain constant at the small signal test performance values, after compensating for the interconnect losses, up to the tested power level of 20W thus validating the design of 20W Receive protection switch with on-chip current paralleled, stacked FET technique.

Fig. 5.17 shows the power sweep test results of the 20W protection switch.

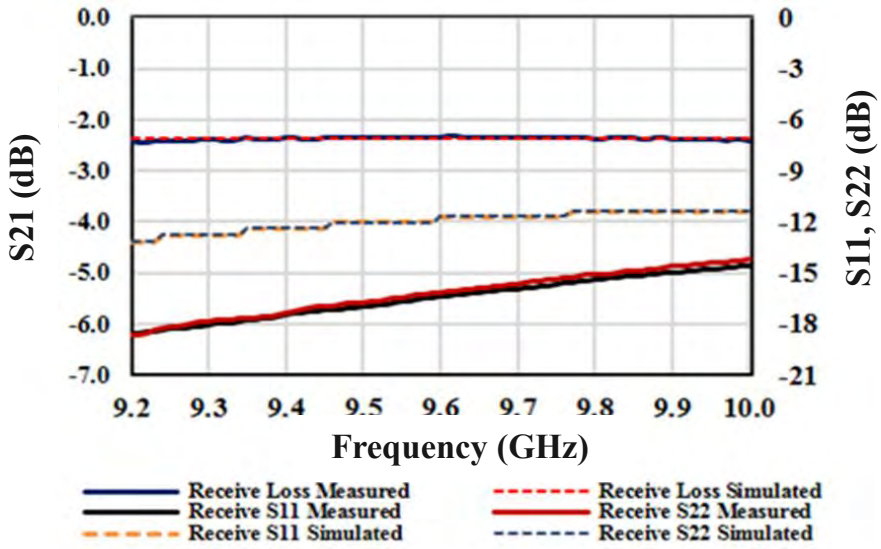

Figure 5-16. Measured result of 20W switch in Receive mode

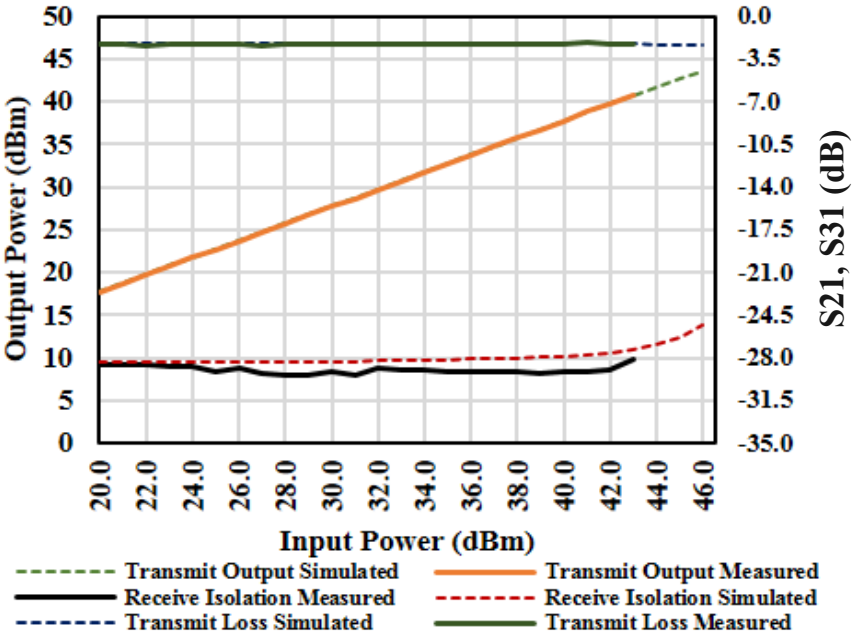

Figure 5-17. Power sweep test results of 20W switch

5.4 Design and Realization of 200W GaN T/R switch (GH25 GaN process of UMS)

Following the design approach presented in 3.2.2.2, in the present work, a shunt resonant HEMT switch enabled DPDT configuration is employed for realizing high power T/R switch while employing the technique of *impedance transformation along with on-the-chip coherent current distribution* to design a 200W switch. The design has been carried out on standard commercially accessible 0.25µm GaN pHEMT process (GH25-UMS foundry). Conventionally, the impedance transformation technique is employed to increase the power handling capability of "OFF" FET switches by placing the shunt FET at a lower impedance point. As the shunt FET operates at a lower impedance point, the voltage swing generated across its drain to source channel reduces, resulting in high power handling capability of the switch. *However, in the proposed technique, the step-down impedance transformation is employed to improve the receive path loss, while power handling capability is achieved by on-the chip coherent current distribution.*

5.4.1 High Power Switch Element

The GH25-10, 0.25µm GaN pHEMT process from UMS (GH25-10), has typical parameters like Vp=-3.5V, $V_{DS\ max}$=90V @ V_{GS}=-20V, $I_{DSS\ typ.}$=825mA/mm. For this process, the OFF state linear power handling capability is 20W, but needs control voltages of 0/-20V. Whereas, when used in ON state the linear power handling capability, for widest 800 µm single shunt FET, is 3.1 W and the switch can be controlled using 0/-4V only. The typical R_{DSON} and $R_{DS\ OFF}$ are 6.0 and 1000Ω respectively for this device. It can be seen from Fig. 3-18, this 3.1W power handling capable GaN FET device is employed to realize a 525 W T/R Switch with coherent current distribution across 8 identical devices having transmit loss of 0.15 dB with receive isolation of 35 dB and receive loss of 1.6 dB. However, as the no. of devices paralleled are increased, the power handling capability is significantly enhanced, but the receive path loss also increases significantly due to reduced $R_{DS\ OFF\ eff.}$ **Hence a novel impedance transformation technique along with on-chip coherent current distribution is devised to improve the receive path loss without significantly affecting the power handling capability.** FET stacking technique can be used for reducing the receive path loss. However, as the switch is handling large powers, the impedance transformer technique provides reduced voltage swings along with

improved receive path loss. 50Ω to 25Ω transformation improves receive loss by 0.8 dB, with 3dB reduction in power handling, which otherwise would have been 6 dB if half the no. of devices are paralleled. Fig. 5.18 shows the layout of 8 FET paralleled GaN T/R switch.

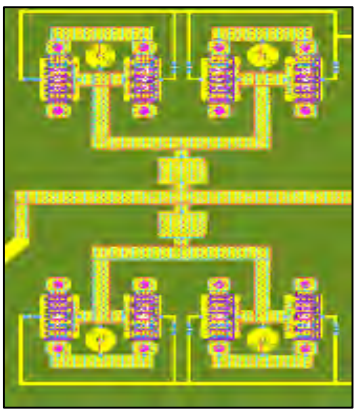

Figure 5-18. 8-FET Paralleled GaN T/R switch

5.4.2 Input and Output Hybrids:

Conventional miniaturized branched line hybrid occupies large MMIC die area. Spiral hybrid and lumped element hybrids cannot handle the high power of 200W due to finite width of air-bridges employed in inductors. Additionally, the λ/4 transformer is large at S-band. Hence to design inductor less, high power, miniaturized, impedance transforming quadrature hybrid with a perfect match on all ports, modified quasi lumped hybrid, as detailed in section 4.2.8.1, is designed and analyzed. Figure 5.19 shows the layout of 50Ω to 25Ω impedance transforming quadrature hybrid used at input and output of the balanced T/R switch.

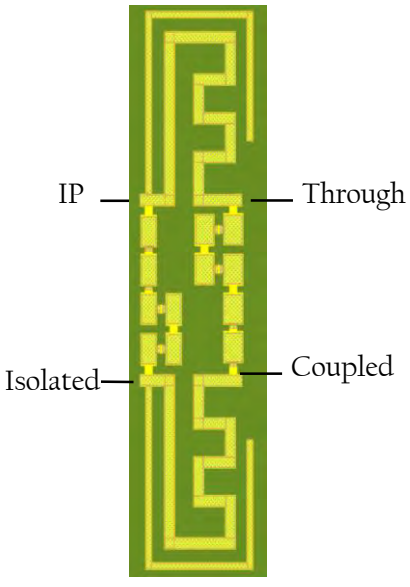

Figure 5-19. Layout of impedance transforming quadrature hybrid

5.4.3 Integrated 200W Receive Protection Switch

The impedance transforming input hybrid, high power switch element and non-transforming output hybrid are integrated. Fig. 5.20 and Fig. 5.21 show the schematic and layout of the 200W GaN T/R switch. Table 5-3 shows the component values of the switch. The complete structure is simulated using harmonic balance analysis in CAD tool, Advanced Design System (ADS), with non-linear FET device from the foundry.

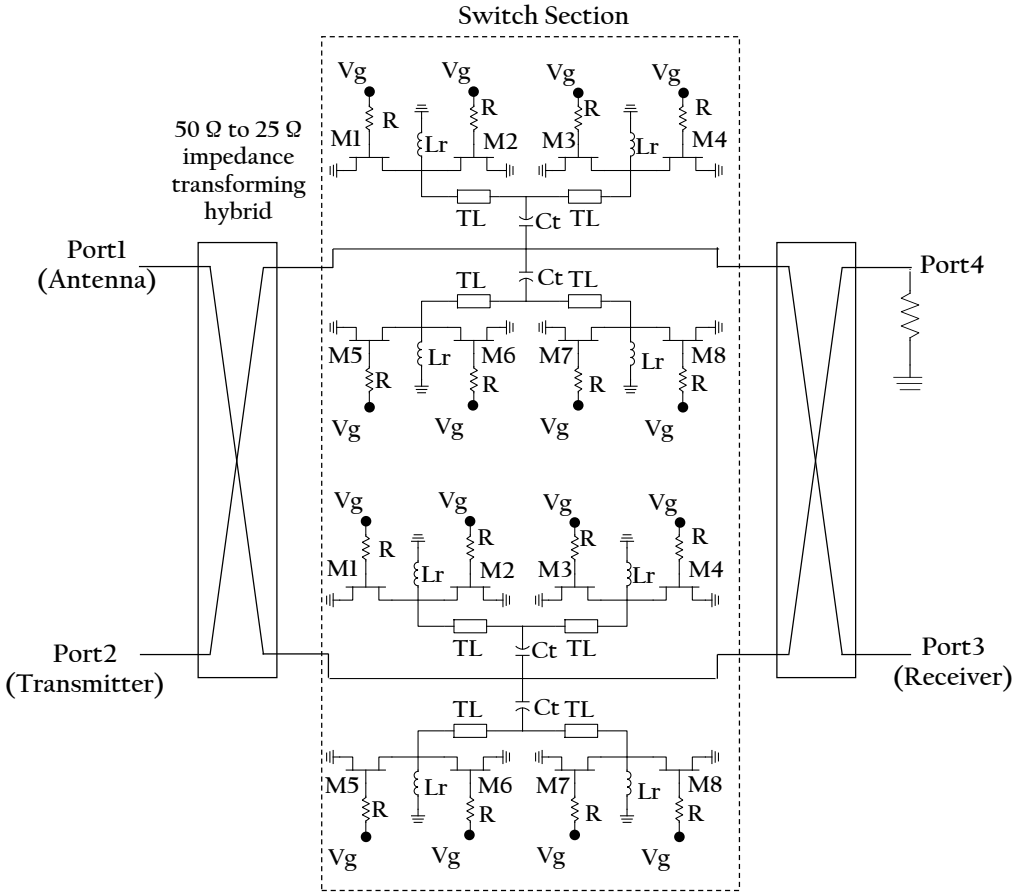

Figure 5-20. Schematic of 200W high power T/R Switch

TABLE 5-3.

Component values of proposed 200W switch

M1-M16	100 X 8 μm
Lr1, Lr2, Lr3, Lr4	3.2 nH
Ct1, Ct2, Ct3, Ct4	9 pF
R	4 kΩ
TL	50Ω, 25^0

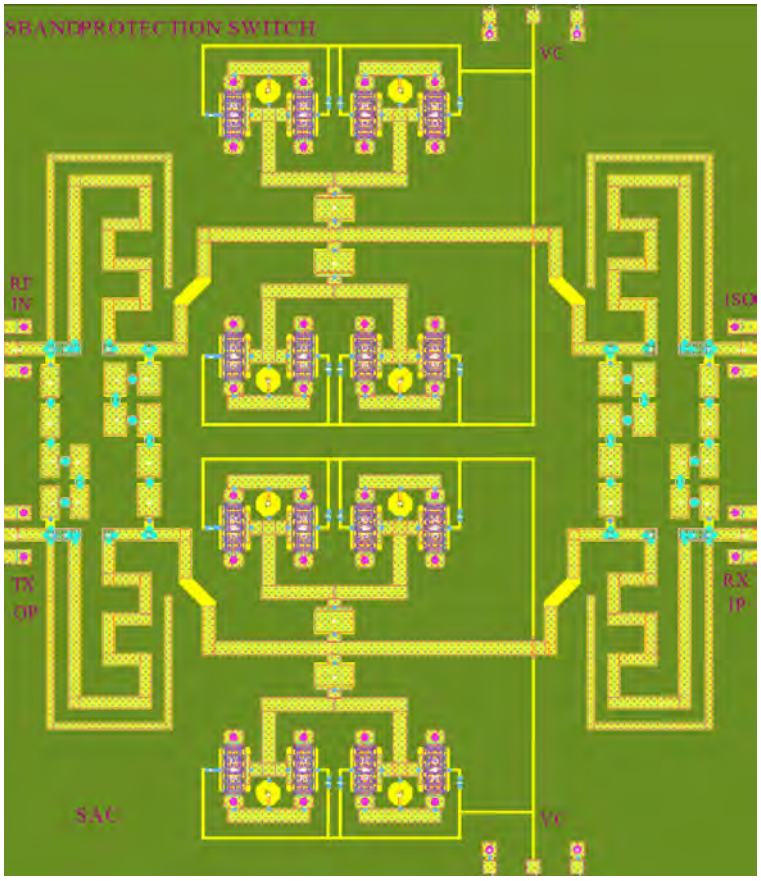

Figure 5-21. Layout of 200W GaN T/R Switch

Fig. 5-22 shows the current distribution across stacked FETs, for the upper branch, with 200W input. The simulated currents are less than 800mA and its variation across FETs is less than 10%.

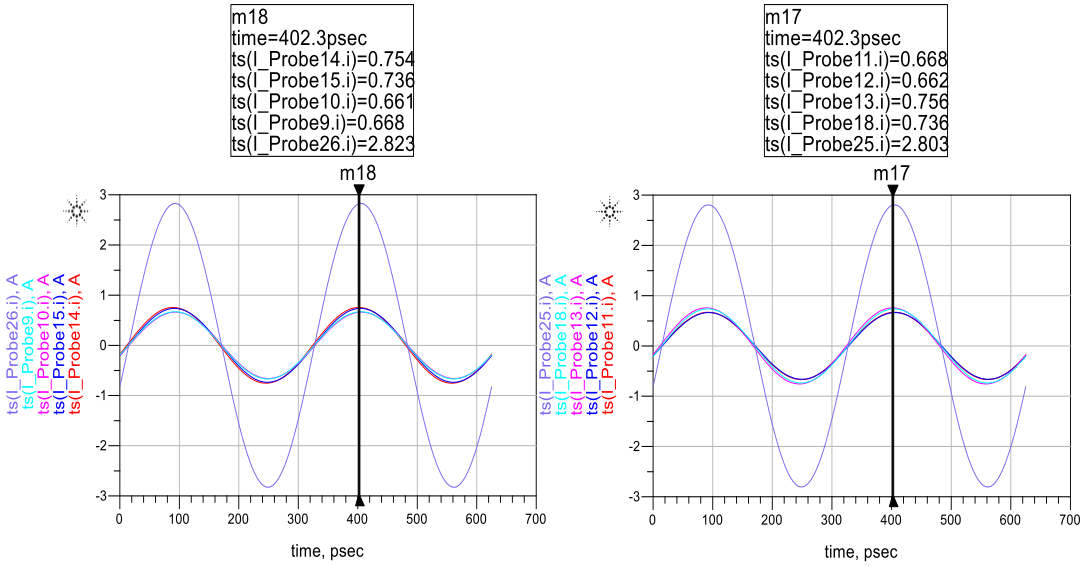

Figure 5-22. Upper branch current distribution across FETs at 200W (+53 dBm) (a) Lower Arm (b) Upper arm

Figure 5.23 shows the simulated results of T/R switch in transmit mode. Transmit loss and receive isolation are better than 0.75dB and 38 dB respectively. Figure 5.24 shows the simulated results of the receive path of T/R switch. Insertion loss in receive mode is < 2.4dB. This includes the loss of input and output hybrid and switch losses. Simulated input and output return loss are better than 15dB across the operating bandwidth.

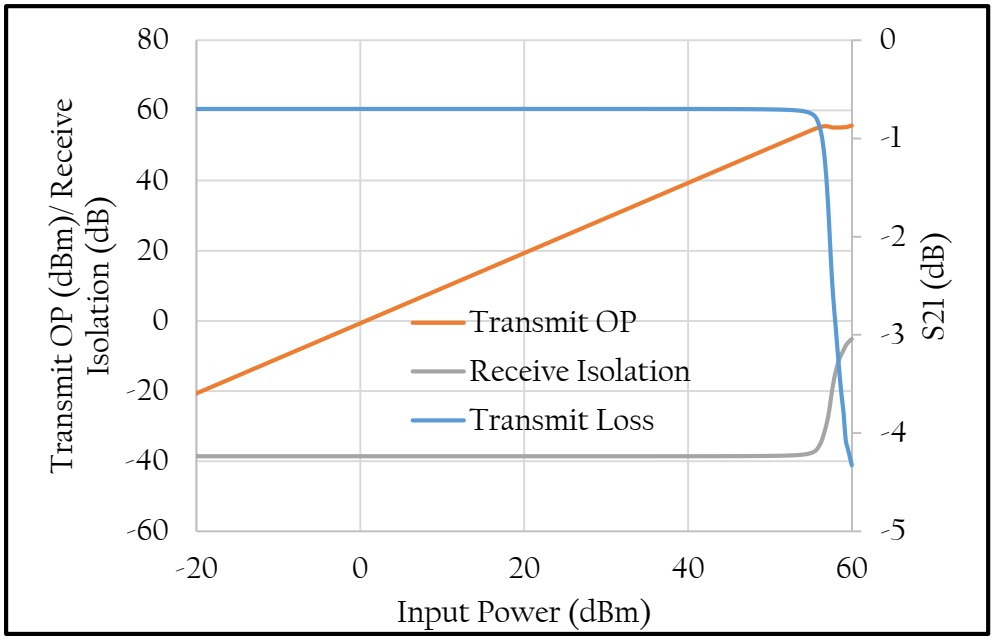

Figure 5-23. Simulated results of 200W T/R switch in Transmit mode

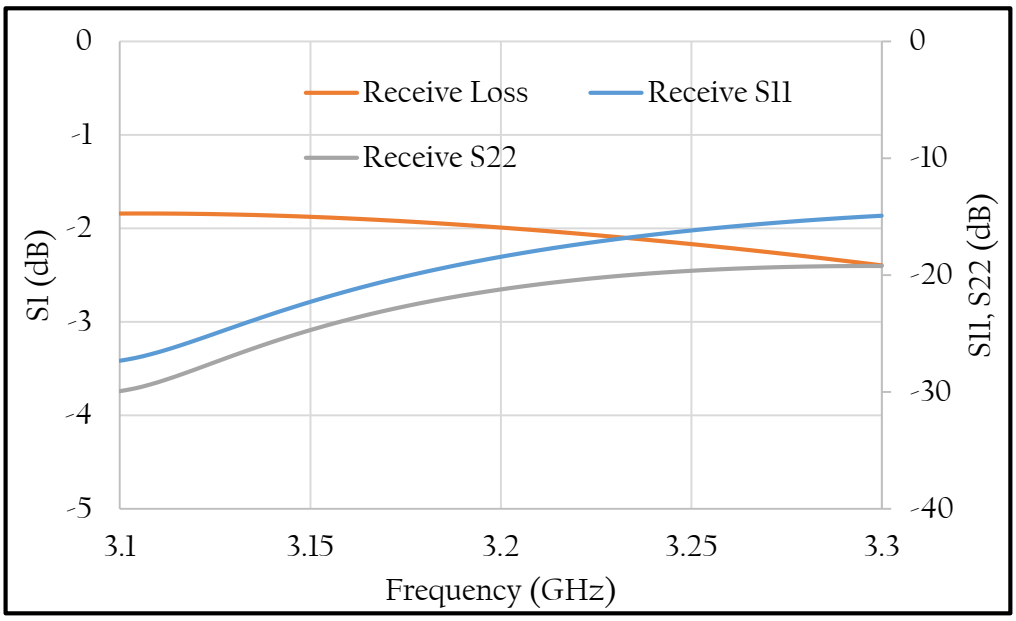

Figure 5-24. Simulated results of 200W T/R switch in Receive mode

5.5 Conclusions

- ✓ Utilizing the proposed modified lumped element 50Ω to 25Ω impedance transforming quadrature hybrid, over 3200 ± 40 MHz, and employing the impedance transformation technique along with on-the-chip coherent current distribution, 200W GaN T/R switch using 0.25 µm GaN process (GH25 of M/s UMS) has been designed, analyzed and simulated. The transmit loss and receive isolation are better than 0.75dB and 38 dB respectively. Insertion loss in receive mode is < 2.4dB which includes the loss of input and output hybrid and switch loss. Simulated input and output return losses are better than 15dB across the operating bandwidth.
- ✓ 20W absorptive receive protection switch MMIC is designed employing on-the-chip current distributed, resonant shunt stacked FET switch configuration and fabricated using low power, low noise OMMIC D01PHS 0.13-µm GaAs pHEMT process. This novel MMIC provides protection up to 20W and exhibits transmit and receive losses of 2.0 dB and 2.3 dB respectively over 9.3-9.9 GHz.
- ✓ 10W Transmit/ Receive switch MMIC is designed employing on-the-chip current distributed, resonant shunt FET switch configuration and fabricated using low power, low noise UMS PH25 0.25-µm GaAs pHEMT process. This novel MMIC has been tested to 10W for power handling capability and exhibits transmit and receive losses of 1.0 dB and 2.3 dB respectively and high power isolation of 28 dB over 9.3-9.9 GHz.

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Chapter: 6

MMIC Low Noise Amplifiers

6.0 Introduction

Low Noise Amplifiers (LNAs) play an important role in extracting signals from noise and are a vital part of the receiver in any microwave payload. When it comes to space applications, Monolithic Microwave Integrated Circuit (MMIC) approach is always preferred over discrete hybrid based design due to its enormous benefits like excellent reproducibility, high reliability due to less no. of interconnects, superior high frequency performance due to less parasitics, small size and light weight. MMIC is a microwave circuit in which the active and passive components are fabricated on the same semiconductor substrate. Since LNA is the first amplification stage in a receiver after requisite receiver protection circuitry, RF input signal level is low enough, such that the active device operates in a completely linear region. These are basically small-signal amplifiers optimized such that they add minimal noise to the RF input signal. Techniques such as series inductive feedback allows the amplifiers to have a good input match, as well as a very low noise figure. LNAs can be designed using standard S-parameter techniques with input matching to ensure optimum noise performance.

Figure 6-1 shows the block representation of an amplifier with signal & noise at its input and output where 'N_A' is the noise added by the amplifier given by $kT_{eq}BG$.

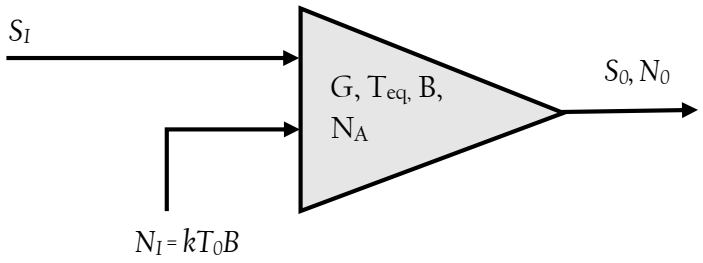


Figure 6-1. Block representation of an amplifier with Signal and Noise at Input and Output

Noise Figure is the figure of merit, which is used to quantitatively determine the noise performance of an LNA. Noise Figure 'F' is given by:

$$F = \frac{S_I/N_I}{S_0/N_0} \quad (6.1)$$

$$= \frac{N_0}{GN_I} \quad (6.2)$$

$$= \frac{GN_I + N_A}{GN_I} \quad (6.3)$$

$$= \frac{GkT_0B + GkT_{eq}B}{GkT_0B} \quad (6.4)$$

$$= 1 + \frac{T_{eq}}{T_0} \quad (6.5)$$

where, $N_0 = GN_I+N_A$ and T_{eq} is the noise equivalent temperature of the amplifier, and T_0 is the ambient temperature.

In a two-stage amplifier shown in Fig. 6-2, the overall noise figure is determined from the noise figures of both the individual stages and associated gains using the Friis formula [1], as given below:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} \quad (6.6)$$

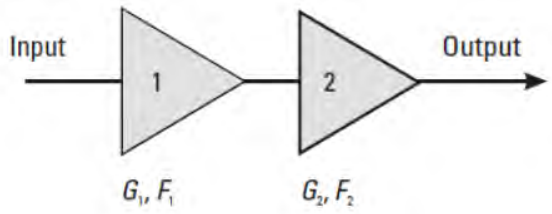


Figure 6-2. Cascaded Two-stage Amplifier

It can be seen from the Friis formula that the noise figure of the first stage directly affects the cascaded noise figure of the two-stage amplifier, whereas the noise figure of the second stage is reduced by the gain of the first stage. Hence, to achieve a minimum noise figure in a two-stage amplifier, the first stage must be designed for the lowest possible noise figure and the highest possible gain.

6.1 Choice of Component Technology and Foundry

The primary factor which governs the DC and RF performance of semiconductor devices is fundamentally the substrate from which the devices are fabricated. Table 6-1 presents a brief overview of the material properties of most commonly used semiconductor substrates and their current technology status [2]. Lot of technology advancements have taken place in the field of semiconductor devices. This field, which was predominantly governed by silicon, is seeing new dimensions with the introduction

of III-V semiconductors, in particular Gallium Arsenide (GaAs), which is now a workhorse semiconductor for various applications. The dominance of GaAs as the primary semiconductor material is due to its two key advantages over silicon for MMICs: (1) GaAs has higher saturated electron drift velocity, resulting in faster devices; (2) GaAs has high resistivity, making it a suitable substrate for microwave passive components. GaAs High Electron Mobility Transistor (HEMT) based LNAs offer state-of-the-art performance in terms of noise as well as high frequency performance. New wide bandgap semiconductor materials, such as Gallium Nitride (GaN), are characterized by a much higher breakdown voltage, and hence have higher power handling capability. GaN HEMTs based LNAs are becoming an increasingly popular choice when higher power handling, linearity and robustness are required without compromising the noise performance. Even though Indium Phosphide (InP) material has number of excellent properties like higher saturated drift velocity and higher electron mobility than either GaAs or Si, it is not widely used due to its non-optimum material characteristics, high leakage current due to low barrier, less resistivity than GaAs due to smaller band gap etc.

Table 6-1
Characteristics of commonly used semiconductor materials [1]

Material	Electron Mobility (cm^2/Vs)	Peak Velocity ($\times 10^7$ cm/s)	Frequency Range (GHz)	Noise Figure	Gain	Comments
Si	900–1,100	0.3–0.7	< 20	Moder-ate	Moderate	Mature process; 12-in. wafers
SiGe	2,000–300,000	0.1–1.0	10–40	Lower	Better	Benefits from Si; 6-in. wafers
SiC	500–1,000	0.15–0.2	15–20	Poor	Lower	4-in. wafers
GaAs	5,500–7,000	1.6–2.3	>75	Lower (F_{min} at 26 GHz = 1.1 dB)	Higher (G_{ass} at 26 GHz = 9.0)	Less mature than Si; 3-, 4- and 6-in. wafers
GaN	400–1,600	1.2–2.0	20–30	Poor	Lower	Less mature than GaAs; V_{br} > 100V; 2-in. wafers
InP	10,000–12,000	2.5–3.5	>115	Lower (F_{min} at 26 GHz = 0.9 dB)	Higher (G_{ass} at 26 GHz = 11.1)	Less mature than GaAs; 2-in. wafers

The next step, once the substrate has been finalized, is to finalize the transistor technology of the foundry that will be used as the active component for getting the requisite DC and RF performance characteristics. HEMTs offer excellent noise performance since the electrons are held within a channel, and are confined very closely to the heterojunction and form a two-dimensional electron gas. This two-dimensional (2D) electron gas is confined away from the lattice atoms so they will not collide with them, which reduces scattering and hence, their shot noise contribution. Hence, pseudomorphic HEMTs (pHEMTs) and Metamorphic HEMTs (mHEMTs) are the most promising candidates for designing monolithic LNAs. *For this current work, GaAs pHEMT and GaN HEMT based MMIC LNAs have been designed owing to its superior performance characteristics, as discussed above.* Details of the UMS & OMMIC foundry process chosen for designing LNAs is given in Table 6-2.

Table 6-2
UMS & OMMIC MMIC Technologies for LNA design

Process	***OMMIC MMIC Technology***	***UMS MMIC Technology***	
	D01PH	***PH25***	***GH25-10***
Active Device	pHEMT	pHEMT	HEMT
Power Density	600mW/mm	250mW/mm	4.5W/mm
Gate Length	130nm	250nm	250nm
Saturated Drain Current 'Idss'	800mA/mm	1000mA/mm	500mA/mm
Breakdown Voltage	12V	> 6V	> 100V
Cut-off Frequency	105GHz	90GHz	30 GHz
Gm max	600mS/mm	560mS/mm	300mS/mm
Noise/Gain	1dB/7.5dB @ 30GHz	0.6dB/13dB @ 10GHz	1.8dB/11dB @ 15GHz

6.2 LNA Design Topologies

The aim of an LNA design is to achieve simultaneously the following features: low noise figure, unconditional stability, low power consumption, good input and output return losses and a gain high enough to make negligible noise contribution to the subsequent receiver stages. Various amplifier design topologies are given in Table 6-3. *In this work, single-stage and two-stage GaAs HEMT LNAs have been designed and fabricated at X-Band and two-stage GaN HEMT LNA has been designed at S-Band, having reactively matched common source configuration with inductive degeneration.*

Table 6-3
Comparison of the MMIC amplifier design topologies [3]

Amplifier Type	Advantages	Disadvantages	Remarks
Reactively matched	Best gain per stage, noise figure and output power	Difficult to control the input and output VSWR. Poor gain flatness when cascaded. Difficult to achieve unconditional stability. Sensitive to process variations	Typically, 20% bandwidths at any centre frequency.
Lossy matched	Good VSWRs and gain flatness. Broadband design, and readily cascadable.	Poor Noise Figure, Reduced gain per stage compared with the reactively matched amplifier.	Octave bandwidths readily achievable. Not suited for LNAs.
Feedback	Excellent gain flatness over a wide frequency range, good stability, and less sensitive to process variation	Average Noise figure and significantly reduced gain. Tends to need large gate-widths, leading to high DC power.	Multi-octave bandwidths readily achievable. Not suited for LNAs.
Distributed	Ultra-wide bandwidths achievable (more than one decade). Good VSWRs easy to cascade.	Low gain, average noise figure and limited output power. High DC power. Large total gate-width required.	Multi-decade bandwidths readily achievable. Not suited for LNAs.
Actively matched	A simple topology for broadband amplifiers at lower frequencies. Small chip size.	Poor noise figure and high DC power requirement.	Multi-octave bandwidths but used at lower frequencies. Not suited for LNAs.

6.3 LNA Design Methodology

Design steps for realizing a reactively matched MMIC based LNA with common source configuration are as follows:

6.3.1 Selection of Device

The first and foremost step in LNA design is to determine device size i.e. unit gate width and no. of gate fingers. Device size will affect bandwidth, DC power consumption, noise figure, and gain of LNA. In order to determine the optimum device

size, small signal and noise performance of several transistors with varying unit gate width and number of gate fingers is determined using a circuit simulator like Advanced Design System (ADS), having the requisite MMIC Process Design Kit (PDK). As device size increases, minimum noise figure (NF_{min}) increases, but for smaller device size, optimum source impedance required for noise match approaches the edge of the Smith chart, making it difficult to attain low noise match. Thus, device size is chosen as a compromise between the two, such that it offers low noise figure, enough gain, along with the ease of input noise matching.

6.3.2 Device Biasing

Active device bias point and load resistance depends on the circuit application. Typically, LNAs are biased at 10-20 percent of the drain saturation current (I_{DSS}) as a trade-off between gain and noise figure. It is preferable to bias LNAs near pinch-off to achieve optimum noise performance; however sufficient gain is also required to reduce the noise contribution of subsequent amplifier stages. Gain & linearity of LNA improves by large drain current, but at the expense of noise figure (NF_{min}). Hence, drain current is chosen to achieve less noise figure, along with sufficient gain. Reducing drain-to-source voltage (V_{DS}) will decrease DC power consumption, but the drain voltage must be high enough for the device to operate in its saturation region, else in the linear or knee region, the drain current rises linearly with the drain voltage. Each device is biased individually to prevent any feedback path from the bias circuit, which may cause instability.

6.3.3 Stability

Once the device size and operating point have been chosen, and bias networks have been designed, the next step is to stabilize the LNA. Series inductive feedback has been used to bring optimal noise match and conjugate input matching closer. Along with bringing the optimum noise match and conjugate input match closed, series inductive feedback also aids to stability. Resistors are generally required either in series or in parallel to the active device to ensure unconditional stability of the circuit. In most of the MMIC LNAs, resistors are used in the output side, so that there is minimal degradation of the noise performance.

6.3.4 Matching Network Design

Reactive matching networks are generally used for MMIC LNA designs to minimize the losses associated with the matching networks. For LNA input match, there

is an optimum reflection coefficient 'Γ_{opt}' to obtain the minimum noise figure 'NF_{min}'. When the active device is presented with Γ_{opt}, the achieved gain is called as associated gain 'G_{ASS}'. Minimum noise match requires that $\Gamma_s = \Gamma_{opt,}$ whereas the condition for minimum input VSWR is $\Gamma_{in} = \Gamma_s^*$. To ensure that minimum noise and conjugate input match appear simultaneously, it is required that $\Gamma_{in} = \Gamma_s^* = \Gamma_{opt}^*$. It is difficult to achieve both low noise and low input VSWR simultaneously since the input reflection coefficient required for simultaneous conjugate match (Γ_{ms}) and for minimum noise (Γ_{opt}) are rarely equal. Mostly, there is a combination of source inductance and load reflection coefficient (Γ_L) that results in $\Gamma_{opt} - \Gamma_{ms}$ concurrence, which leads to minimum noise and minimum input VSWR. But this desirable condition extracts a price by presenting a poor output match and lower power gain. Traditional design techniques include presenting a low noise match at the input ($\Gamma_s = \Gamma_{opt}$), and a conjugate match at the output for low output VSWR ($\Gamma_L = \Gamma_{out}^*$), but since $\Gamma_{in} \neq \Gamma_s^*$, it results in poor input VSWR. In MMIC LNAs, optimum noise and input VSWR performance is concurrently achieved by ***series inductive feedback.*** An optimum input impedance along with series inductive feedback is thus used to achieve best compromise between noise figure and gain, along with ensuring unconditional stability up to cut-off frequency of the active device. Input and output matching networks are realized using passive LC networks at lower frequencies and microstrip lines at higher frequencies.

6.4 Design of X-Band GaAs LNAs

6.4.1 Single Stage Low Noise Amplifier

For realizing a 10W T/R Switch with LNA using PH25 GaAs PHEMT process of UMS, a single stage LNA is designed over the intended band of frequency 9.3-9.9 GHz.

6.4.1.1 Bias Network

Bias network is designed using an inductor choke of 3.17nH and a coupling capacitor of 2.0 pF to provide high impedance at operating RF frequency over DC supply line. A series resistor of 10 Ω is added in bias tee of gate to provide out of band stability. An in series resistor capacitor network of 340 Ω and 5pF is connected from bias to ground near the gate and drain supply pads. This network is used to damp any low frequency oscillation. Fig. 6-3 (a) and (b) show the schematic of the designed gate and drain bias tee network. S-parameter simulation of both the bias network was done using ADS. Fig. 6-4 (a) and (b) shows the S- parameter response of gate and drain bias network respectively.

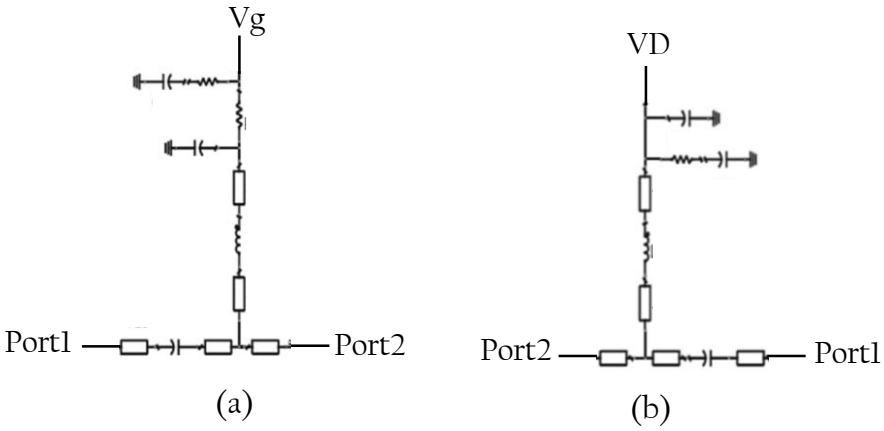
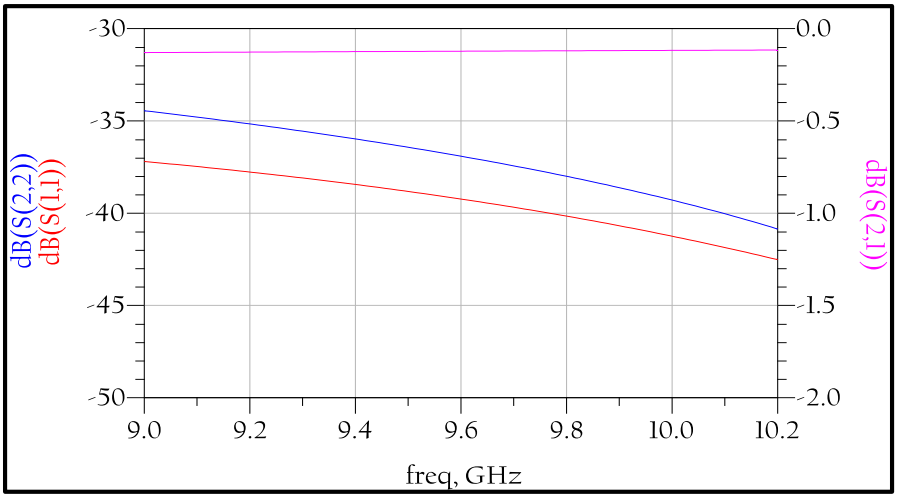
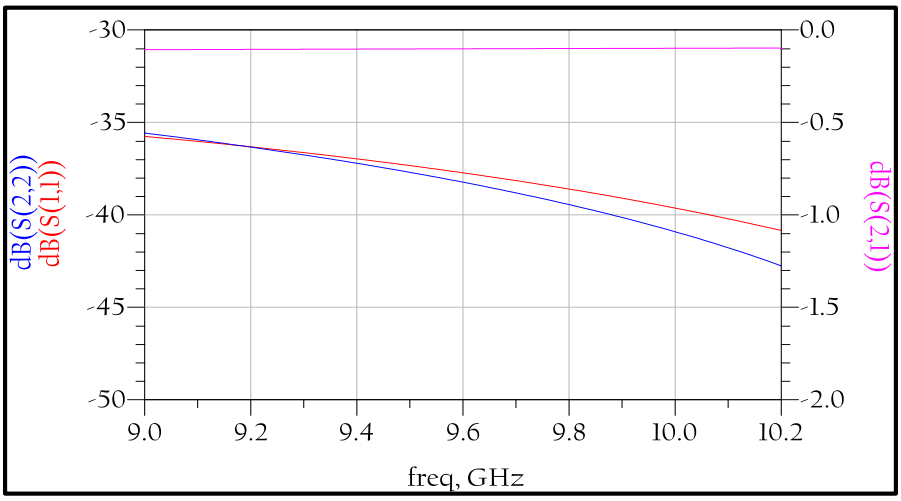


Figure 6-3. Schematic bias tee network.
(a): Gate bias tee (b): Drain bias tee



(a)



(b)

Figure 6-4. Simulation result of bias tee network
(a): Gate Bias tee (b): Drain bias tee

6.4.1.2 Selection of device size

Device sizing and bias are selected to obtain the best NF with required gain. The selection of device periphery and bias is a compromise between gain and NF. Total gate width is 300 µm and is biased at 15 mA i.e., 15% IDSS. 4 numbers of gate fingers are used to achieve the total periphery of 300 µm. Paralleling of gate finger reduces the input gate resistance, and hence improves the noise figure performance of the device.

6.4.1.3 Stability Analysis

Unconditional stability of the FET along with its bias tee network for drain and source is ensured till f_T of the device. All FETs are inherently unstable due to RF feedback from its drain to gate terminal through drain to gate capacitance. There are several methods to improve the stability of the device. This includes adding a series resistor in RF path of gate/drain terminal to reduce the feedback gain of the device, a shunt resistor from gate/drain to ground, inductive feedback from drain to gate terminal and source degeneration technique. In the present work, source degeneration technique is used to unconditionally stabilize the device. This is done by adding a transmission line between the source terminal of the FET and ground. This provides an inductive feed-back from the output terminal of FET to its input. Fig. 6-5 shows the plot for Rollet stability. For a device to be unconditionally stable, Rollet stability criteria, K>1 and Δ<1, has to be meet till the f_T of the device.

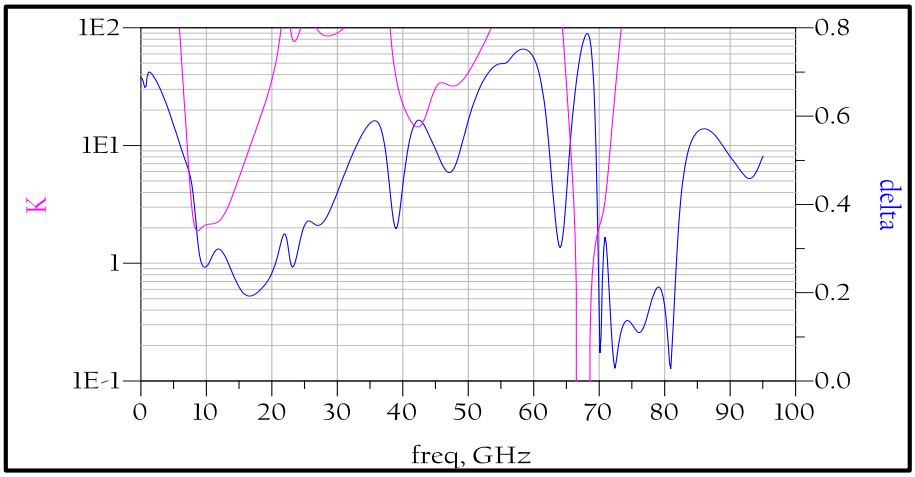


Figure 6-5. Stability factor plot of device with bias-tee network and source degeneration

6.4.1.4 Schematic and layout design and simulation

The schematic diagram of the circuit is shown in Fig. 6-6. As detailed in previous sub-section, source degeneration is employed with inductance realized using transmission line (TL8) to achieve the gain and noise matching, closer to Γ_{opt}, optimal

source reflection coefficient for minimum NF, and real part of the input impedance closer to 50Ω. Conjugate matching is used the output for maximum transfer of power.

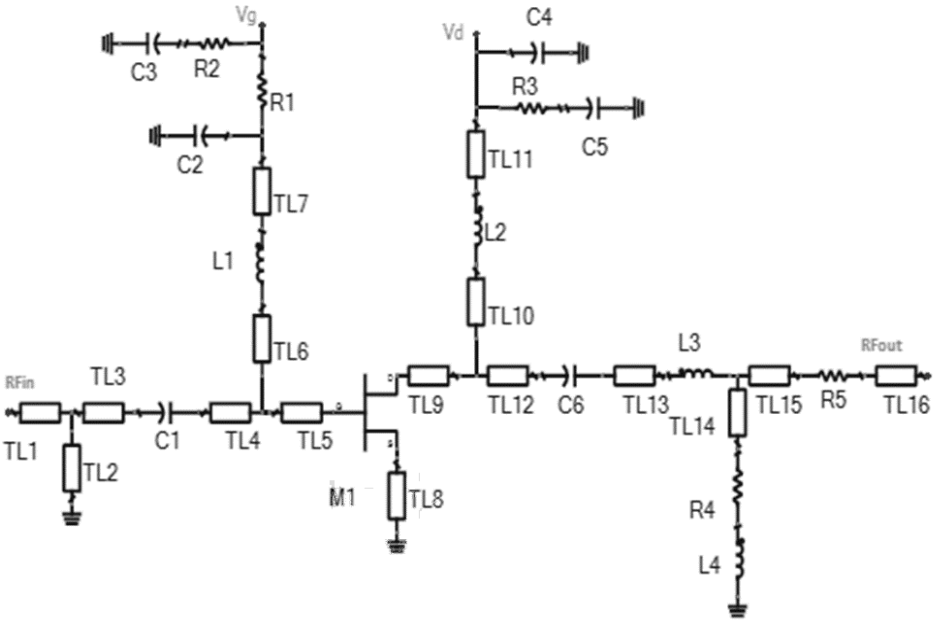


Figure 6-6. Schematic of single stage LNA.

Fig. 6-7 shows the layout of the designed single stage LNA. An electromagnetic simulation of the complete layout was done using ADS and subsequently, co-simulation was done using linear model of FET to analyses the S-parameter of LNA and its noise figure.

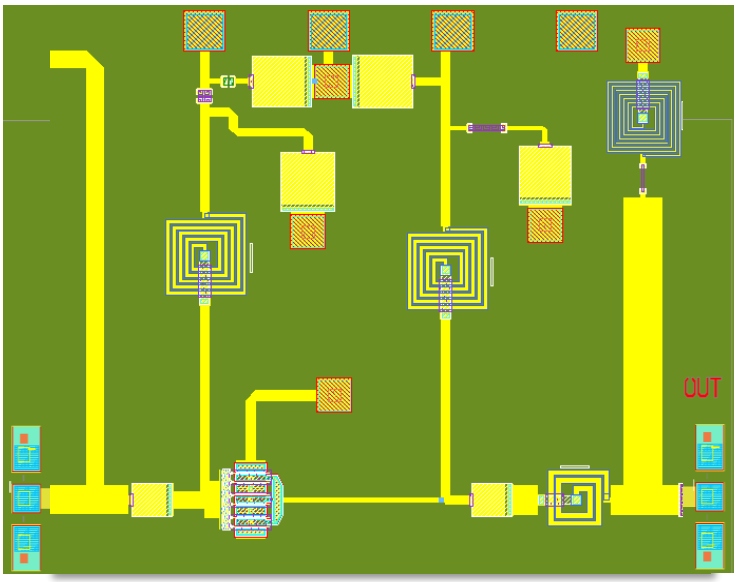


Figure 6-7. Layout of single stage LNA

Figure 6-8 shows the simulated response of designed single stage LNA. Gain is better than 10dB and noise figure across the band is less than 1.0dB. Input and output return losses are better than 16dB.

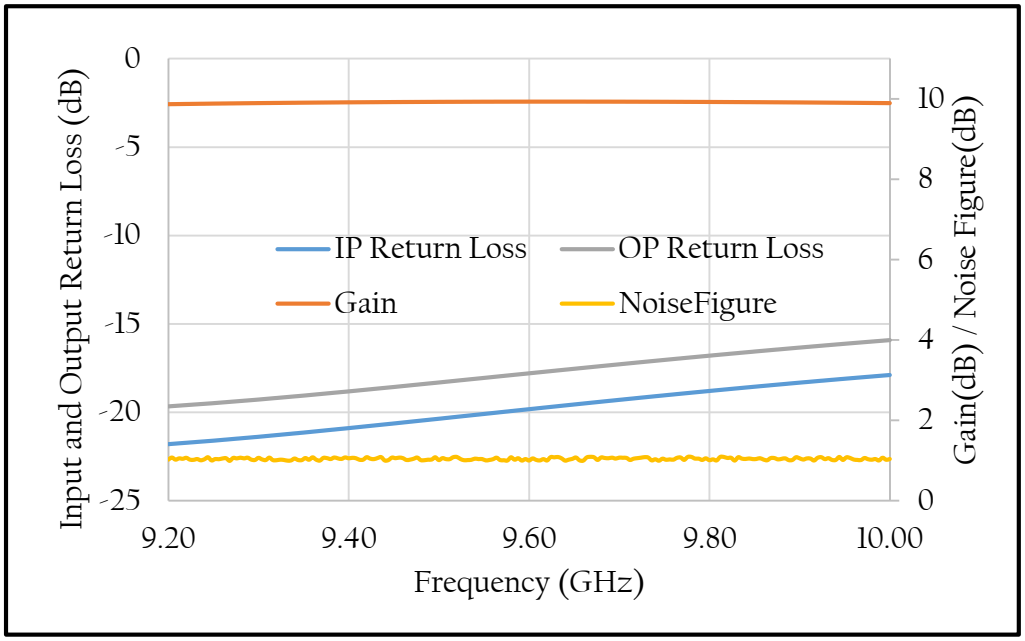


Figure 6-8. EM simulation result of single stage LNA

6.4.1.5 Measurement Results

The design was fabricated using PH25 process of UMS foundry and MMIC was on-wafer tested. Fig. 6-9 shows the on-wafer test result of the fabricated MMIC. Noise figure was measured using Y-factor method with Noise Figure Analyzer. Gain of the MMIC varies from 10.9 dB to 10.5 dB and noise figure varies from 0.9 dB to 0.7 dB from 9 GHz to 10 GHz of frequency. Measured input and out return losses are better than 12 dB and 18 dB respectively.

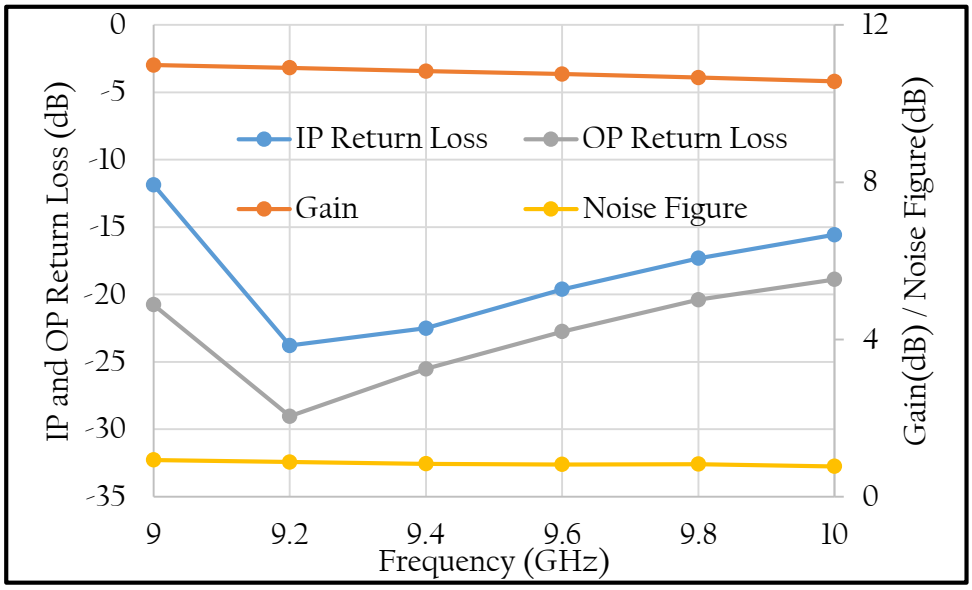


Figure6.9: On-wafer measured result of single stage LNA

6.4.2 Two stage Low Noise Amplifier

Two stage LNA was designed using 130nm psuedomorphic HEMT process, D01PHS of OMMIC foundry. The short circuit current gain frequency, f_T, of the process is 110 GHz. The design process is similar to as explained in the previous sub-section on single stage LNA.

6.4.2.1 Bias Network

Bias network is designed using an inductor choke of 3.0 nH and a coupling capacitor of 4.5 pF to provide high impedance at operating RF frequency over DC supply line. A series resistor of 10 Ω is added in bias tee of gate to provide out of band stability. An in series resistor capacitor network of 150 Ω and 5pF is connected from bias to ground near the gate and drain supply pads. This network is used to damp any low frequency oscillation. Figure 6-10 (a) and (b) shows the schematic of the designed gate and drain bias tee network.

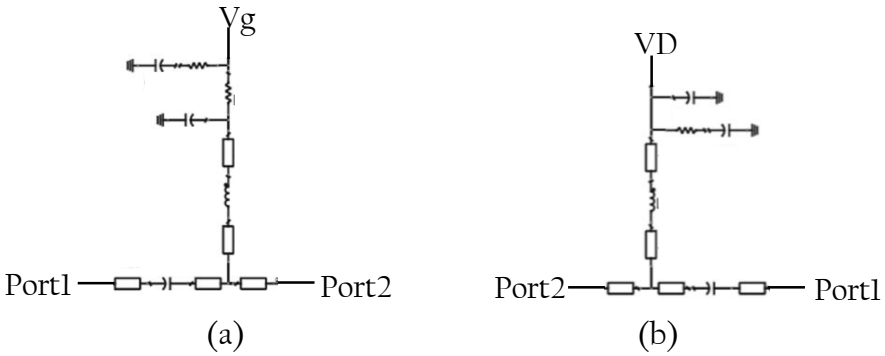


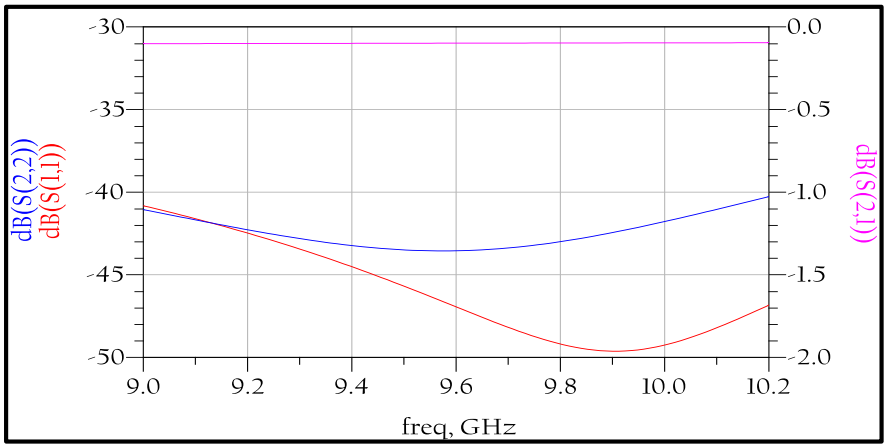
Figure6-10. Schematic bias tee network.
(a): Gate bias tee (b): Drain bias tee

S-parameter simulation of both the bias network was done using ADS. Figure 6-11 (a) and (b) shows the S-parameter response of gate and drain bias network respectively.

6.4.2.2 Selection of device size

Device sizing and bias are selected to obtain the best NF with required gain. As explained previously, selection of device periphery and bias is a compromise between gain and NF. Total gate width is 300 µm and is biased at 20 mA i.e., 15% I_{DSS}. 6 numbers of gate fingers are used to achieve the total periphery of 300 µm. Paralleling of gate finger reduces the input gate resistance, and hence improves the noise figure performance of the device. Device sizing and bias are selected to obtain the best NF

with required gain.



(a)

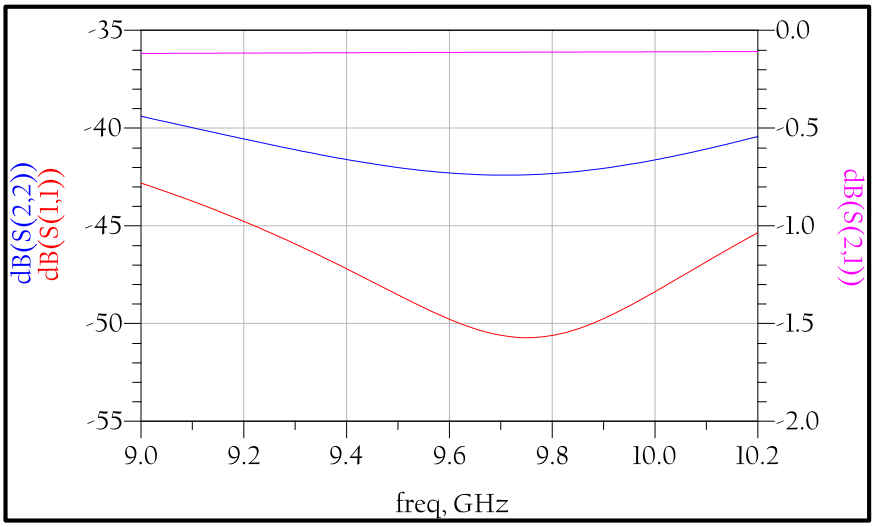


Figure 6-11. Simulation result of bias tee network.
(a): Gate Bias tee (b): Drain bias tee

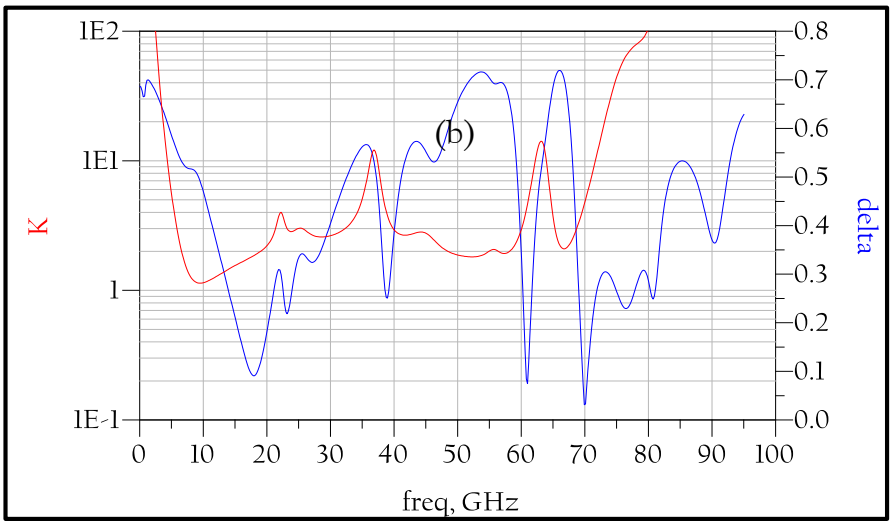


Figure 6.12. Stability factor plot of device with bias-tee network and source degeneration

6.4.2.3 Stability Analysis

Unconditional stability of the FET along with its bias tee network for drain and source is ensured till Ft of the device. Each of the FET along with its bias tee network is made unconditionally stable by adding damping resistors in bias-tee and using inductive feedback by adding transmission line between source terminal and ground. Fig. 6-12 shows the plot for Rollet stability. Unconditionally stability criteria, K>1 and Δ<1, is ensured till 95GHz.

6.4.2.4 Schematic and layout design and simulation

The schematic diagram of the circuit is shown in Fig. 6-13. As detailed in the previous sub-section, source degeneration is employed with inductance realized using transmission line (TL8 and TL22) to achieve the gain and noise matching, closer to Γ_{opt}, optimal source reflection coefficient for minimum NF, and real part of the input impedance closer to 50Ω. The first stage of LNA is matched for minimum noise figure while the second stage is simultaneously conjugate matched at input and output to provide maximum transducer gain.

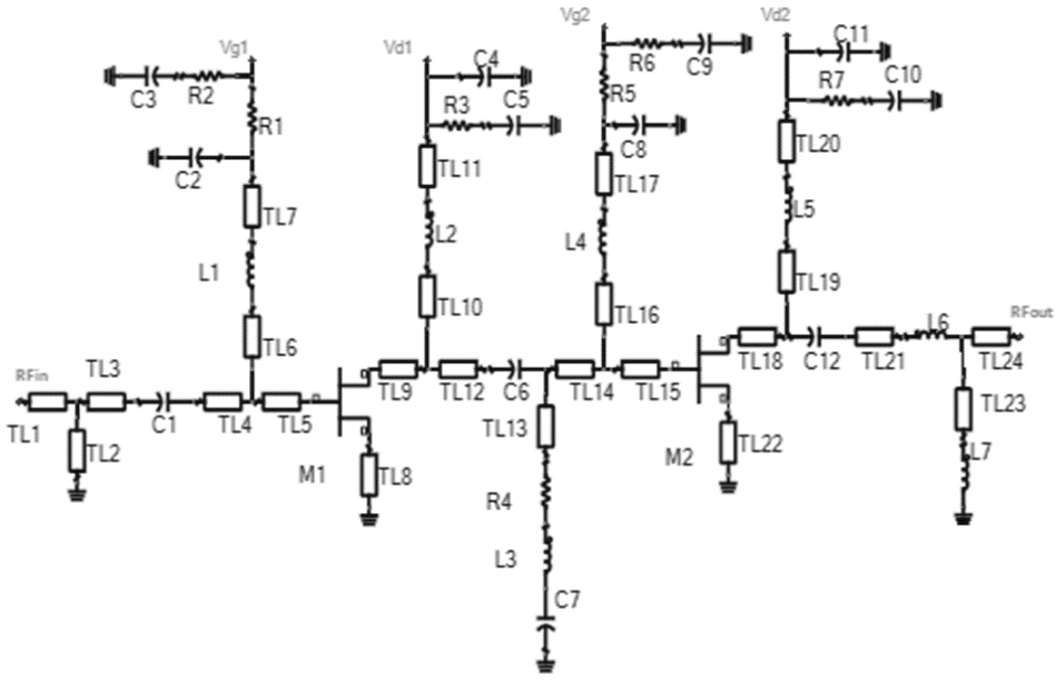


Figure 6-13. Schematic of two stage LNA.

Figure 6-14 shows the layout of the designed single stage LNA. An electromagnetic simulation of the complete layout was done using ADS and subsequently, co-simulation was done using linear model of FET to analyses the S-

parameter of LNA and its noise figure.

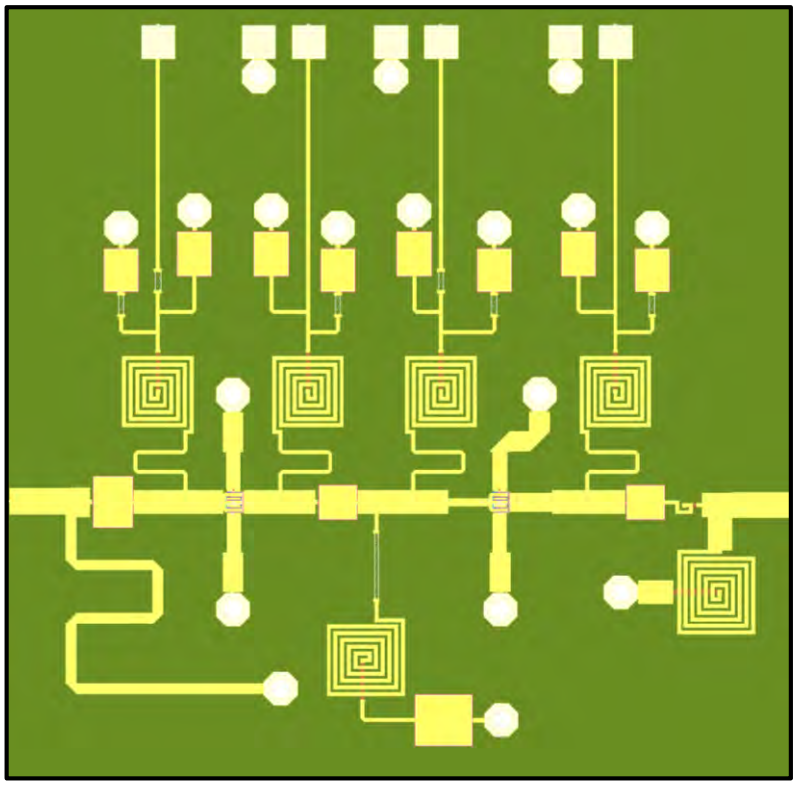


Figure 6-14. Layout of two stage LNA

Figure 6-15 shows the simulated response of designed single stage LNA. Gain varies from 23dB to 25dB, noise figure is better than 1.1dB, input return loss is better than 12dB and output return loss is better than 15dB across 9.0 GHz to 10.2 GHz operating frequency.

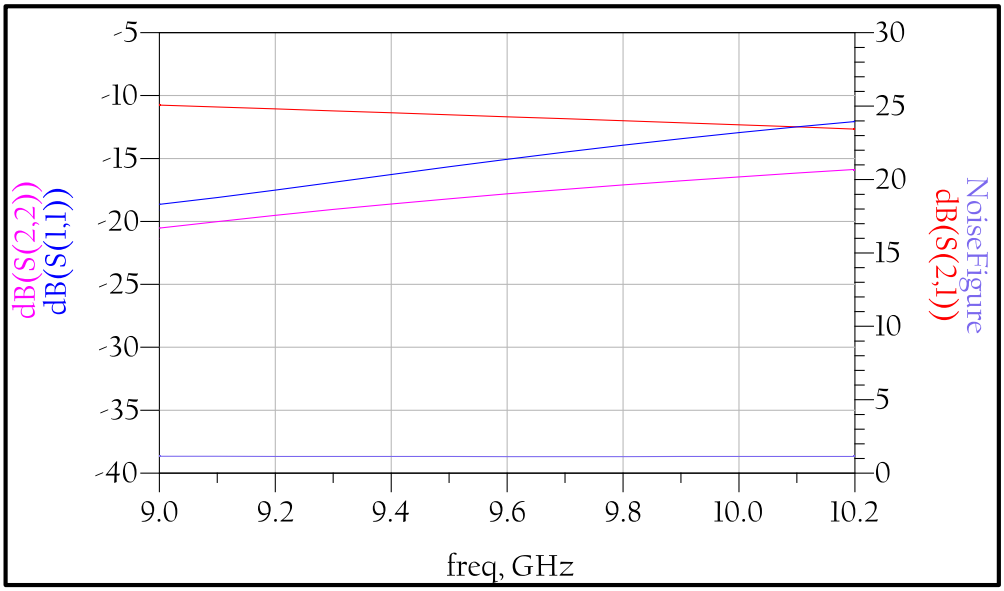


Figure 6-15. EM simulation result of two stage LNA

6.4.2.5 Measurement Results

The MMIC is fabricated and on-wafer tested. Figure 6.16 shows the on-wafer test result of two stage LNA. Noise figure was measured using Y-factor method with Noise Figure Analyzer. Gain varies from 23.1dB to 25 dB, noise figure is better than 1.1dB, input return loss is better than 11dB and output return loss if better than 23dB over 9.0GHz to 10.2 GHz operating frequency.

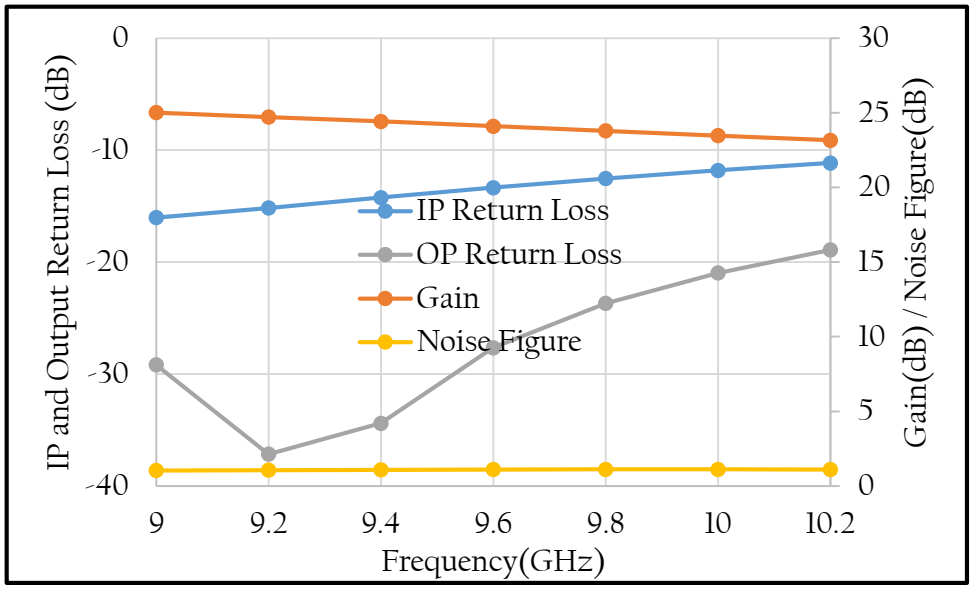


Figure6.16: On-wafer measurement result of two stage LNA.

6.5 S-Band GaN LNA Design

Properties of AlGaN/GaN heterostructure makes the GaN HEMT particularly suitable for high power application along with good noise performance. Due to their wide band-gap compared to GaAs pHEMTs, GaN transistors offer higher power handling, linearity and robustness without compromising noise performance, making them ideal candidate as front-end LNAs for high power transmit-receive modules. Published works on GaN HEMT devices are listed in Table6-4 [4].

This section presents the design of a two-stage S-Band GaN HEMT based MMIC LNA having operating frequency range from 3.1-3.3GHz. This LNA has been designed using 0.25 µm gate length HEMT Technology from United Monolithic Semiconductors (UMS) foundry. UMS GH25-10 is a 0.25µm slanting shape gate foot HEMT process having GaN/AlGaN epitaxy.

Table 6-4
Published GaN HEMT based designs for LNA & Power Amplifier [3]

	BW[GHz]	Gain[dB]	Noise Figure [dB]	Linearity OIP3 [dBm]	Power Consumption [mW]
[3]	2-12	10	3.0	–	15
[4]	4-8	10.9	1.9	24	120
[5]	4-16	14.5	2.0	24	150
[6]	3-7	20	2.3	26	320
[7]	1.2-18	13.3	3.0	–	500
[8]	3-18	20	3	37.8	636
[9]	1-12	15	2.5	34.5	800
[10]	1-25	13	4.6	28.5	900
[11]	0.3-4	18	2	32	1000
[12]	3-16	20	4.0	–	2700
[13]	0.2-8	15	0.9	46.5	6000
[2]	2-8	13	0.35	43	6000
[14]	0.1-20	12.5	5.5	42.6	9000
[15]	1.7-2.3	15	2	49	16500
[16]	2.0	15	2.8	54	24192
[17]	0.5-3	15	2.0	43	–
GaAs *AVAGO*[1]	0.9	17	0.4	35	280
	1.9	18	0.4	35	285
GaAs *SKYWORKS*[2]	0.7-1	18	0.49	34	224
	1.7-2.0	17	0.61	34	224

[1] MGA-633P8 and MGA-634P8 from AVAGO technologies.
[2] SKY67101-396LF and SKY67100-396LF from SKYWORKS.

6.5.1 Bias Network

The bias network determines the amplifier performance over temperature as well as RF drive. Fixed Bias Topology is used in this design for biasing the transistors. Bias to the gate and drain of the transistors is provided through bias decoupling networks which are designed to offer low DC resistance and large RF resistance so that it prevents RF signal from flowing into the DC path. Bias decoupling networks can be realized using either lumped or distributed components. Owing to larger size of quarter wavelength line at the operating frequency, bias networks are designed using lumped components for realizing RF choke, which comprise of a resonator having an inductor and capacitor in parallel, followed by a bypass capacitor to ground, which acts as a short circuit near the operating frequency, in order to bypass RF signal, if any, to ground. An additional on-chip capacitor of 10 pF is used to bypass any low frequency component coming through the supply line, so that it does not interfere with the RF signal. The designed gate and drain bias networks have an insertion loss of approx. 0.1dB.

6.5.2 Selection of device size

Device sizing and bias are selected to obtain the best NF with required gain. The noise characteristics of the 80µm x 8 GaN HEMT device are a minimum noise figure of 0.6dB and a noise resistance of 7.5Ω at 3.2GHz. Series inductive feedback used in both stages reduce the available gain due to negative feedback. Two device stages are required to meet the gain requirement along with low noise figure.

6.5.3 Stability Analysis

Stability resistors are used in shunt in both gate as well as drain bias networks to ensure unconditional stability of the LNA up to the cut-off frequency of the device, so as to prevent it from oscillations for any value of source and load impedances.

6.5.4 Layout design and Simulation

Input and output matching networks are realized using passive LC networks due to lower frequency of operation. An optimum input impedance along with series inductive feedback is used to achieve best compromise between noise figure and input VSWR. Conjugate matching is done for the output match. The circuit layout of two-stage S-Band LNA MMIC is shown in Fig. 6-17.

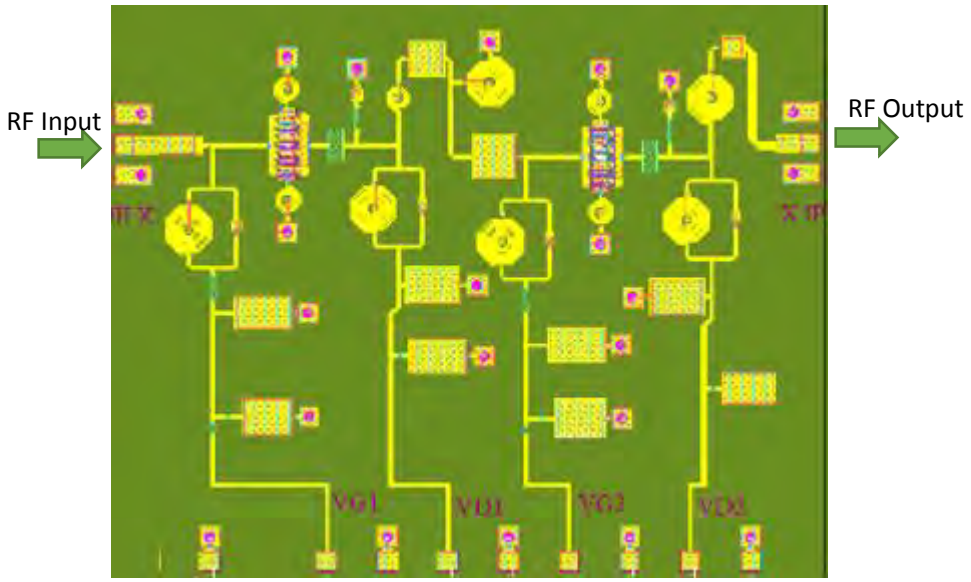
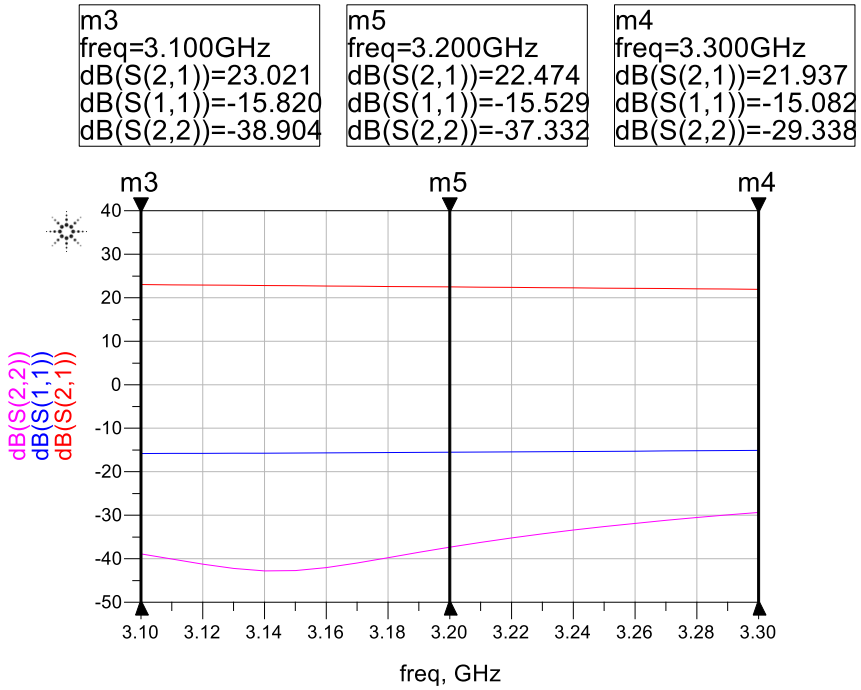


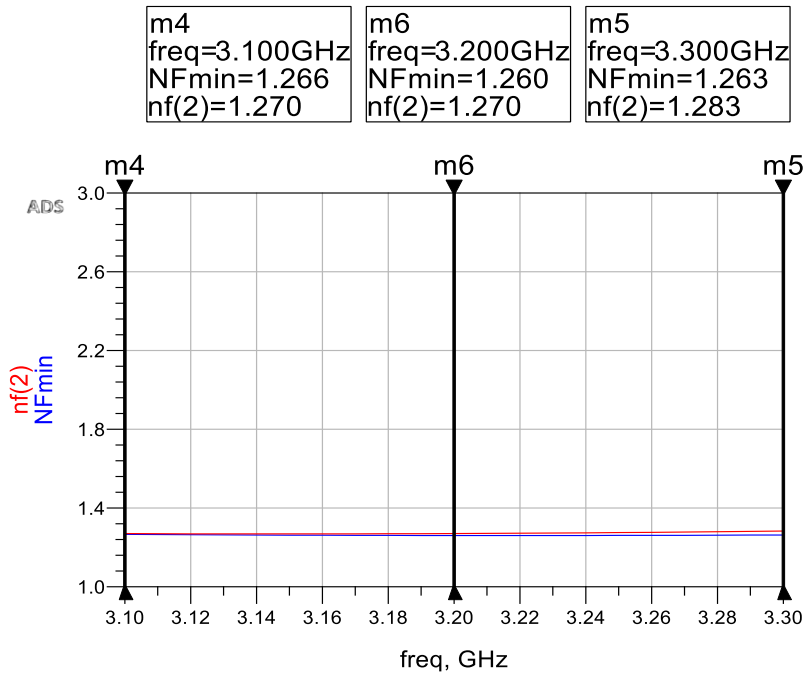
Figure 6-17. Layout of two-stage S-Band MMIC GaN LNA

The two-stage LNA has been simulated using Agilent's ADS Circuit and Electromagnetic (EM) Simulator. EM Simulation has been done for all the circuit components, apart from active device, to analyze the behavior of conductor lines, bends, tees, or any other discontinuities, and also the coupling between elements. Figure 6-18 shows the simulation result of S-Band two stage LNA MMIC. The simulated noise

figure varies from 1.27dB to 1.28 dB across 3.1GHz to 3.3GHz operating frequency. Small signal gain varies from 21.9dB to 23dB with higher gain at the lower end of frequency spectrum. Input return loss is better than 15dB and output return loss is better than 29dB across the required operating frequency.



(a)



(b)

Figure 6-18. Simulation result of S-Band two stage GaN LNA. (a): S-Parameter (b): Noise Figure

6.6 Conclusions

- ✓ A single stage LNA, using UMS PH25 0.25-µm GaAs pHEMT process has been designed, simulated, realized and on-wafer tested. Gain of the MMIC varies from 10.9 dB to 10.5 dB and noise figure varies from 0.9 dB to 0.7 dB from 9GHz to 10 GHz of frequency. Measured input and output return losses are better than 12B and 18dB respectively.

- ✓ A two stage LNA, using D01PHS 0.13-µm GaAs pHEMT process, has been designed, simulated, realized and on-wafer tested. Gain varies from 23.1dB to 25 dB, noise figure is better than 1.1dB, input return loss is better than 11dB and output return loss is better than 23dB over 9.0GHz to 10.2 GHz operating frequency.

- ✓ A two-stage LNA, using UMS GH25-10, 0.25-µm GaN pHEMT process, has been designed and simulated using Agilent's ADS Circuit and Electromagnetic (EM) Simulator. EM Simulation has been done for all the circuit components, apart from active device, to analyze the behavior of conductor lines, bends, tees, or any other discontinuities, and also the coupling between elements. The simulated noise figure varies from 1.27dB to 1.28 dB across 3.1GHz to 3.3GHz operating frequency. Small signal gain varies from 21.9dB to 23dB with higher gain at the lower end of frequency spectrum. Input return loss is better than 15dB and output return loss is better than 29dB across the required operating frequency.

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Chapter: 7

MMIC High Power Transmit/Receive Switches and Receive Protection Switches with integrated Low Noise Amplifiers

7.0 Introduction

The overall receive path loss of high power T/R switch, as described in Chapter 5, is the sum of switch insertion loss in high impedance state, insertion losses of input hybrid and output hybrids. Being a balanced configuration, LNA can be integrated in between the switch and the output hybrid thus removing the effect of output hybrid insertion loss on the overall receive noise figure, as shown in Fig. 7.1, while providing gain. And also, being a balanced structure, it ensures good input and output return losses for the overall structure. With the above approach of being able to design a high power switch, using low noise process, the device supports monolithic integration of LNA along with T/R switch. During transmit operation of T/R switch with LNA, the LNA is switched off, i.e., when high power is being transmitted to antenna. The LNA is switched on during receive mode, i.e. when power is received from antenna, thus providing a low noise figure as compared to stand alone high power T/R switch.

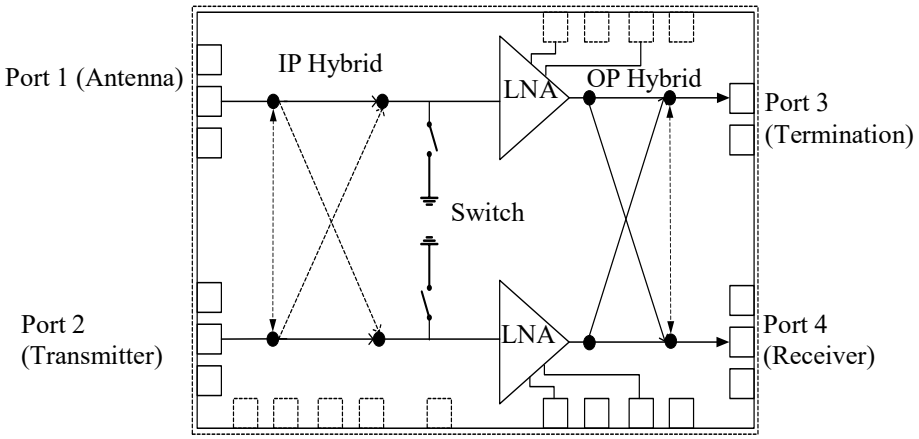


Figure 7-1. Block Schematic of high power T/R Switch integrated with low noise amplifier

7.1 X-Band 10W T/R Switch with integrated LNA

In the present work, the 10W T/R switch with integrated low noise amplifier is designed using 250nm pseudomorphic HEMT process, PH25 of UMS foundry.

7.1.1 Design Approach and Schematic

The input 3-dB quadrature hybrid, on-the-chip coherent current distributed high power switch element in each of the arms of the hybrid, the single stage LNA and the output 3-dB quadrature hybrid are integrated to create 10W T/R switch with LNA.

The already described and tested designs viz., compact spiral hybrid (section 4.2.3), high power switch element (section 5.2.1) and single stage LNA (section 6.4.1) are used for designing the 10W T/R switch with LNA MMIC. Fig. 7-2 shows the schematic of 10W T/R switch integrated with low noise amplifier.

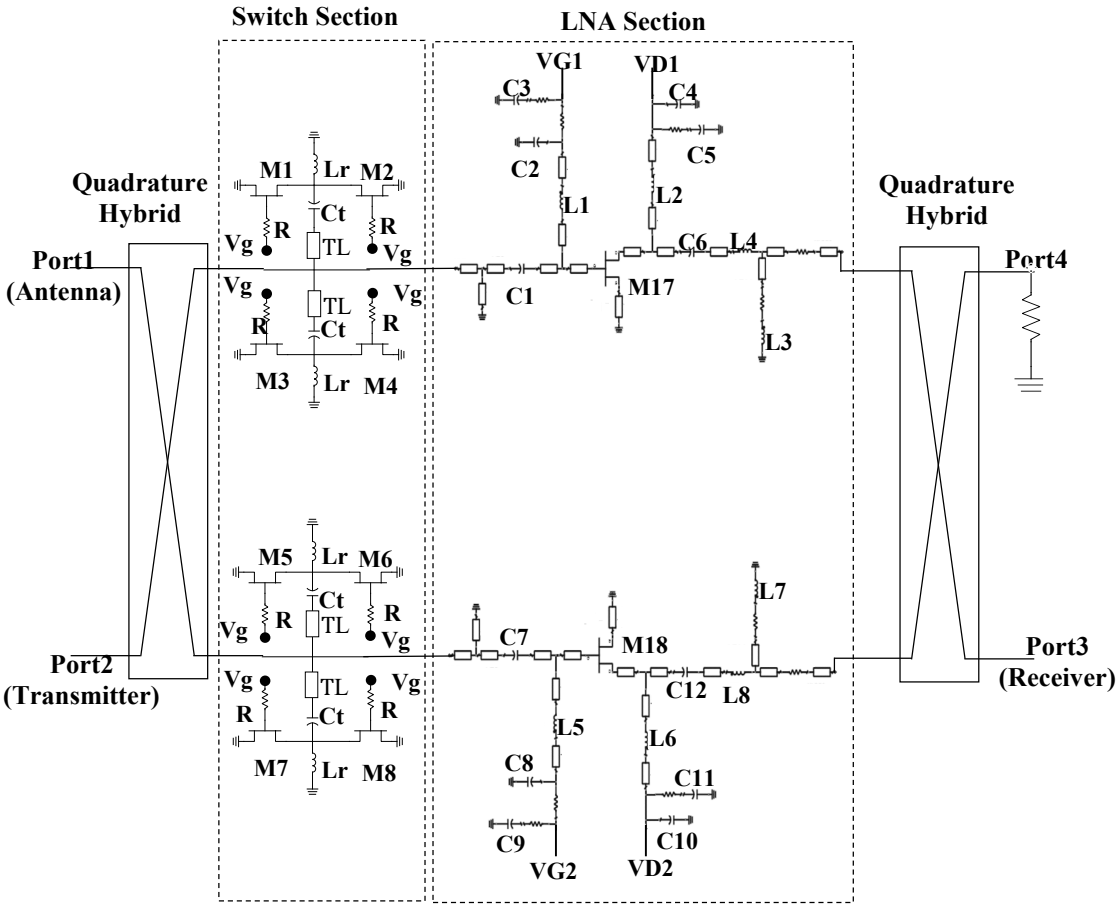


Figure 7-2. Schematic of 10W T/R Switch integrated with LNA

Complete structure is simulated for all the conditions, viz., transmit path loss and isolation assessment during power sweep and frequency sweep for Transmit operation mode and stability, receive path gain and noise figure over frequency sweep for Receive operation mode, using linear and harmonic balance analysis in CAD tool, ADS, with linear and non-linear cold FET device model from the foundry. Fig. 7.3 shows the photograph of realized MMIC.

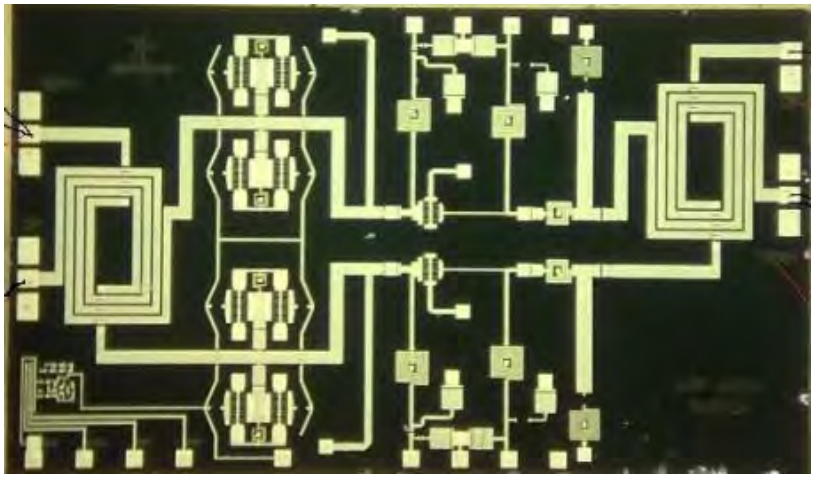


Figure 7-3. Photograph of realized 10 W T/R switch with LNA

7.1.2 Measurement Results

One of the fabricated MMICs is assembled in a test jig, to assess the power handling capability of the designed MMIC.

7.1.2.1 CW Power Sweep Test of 10W T/R Switch with LNA

As the design followed for realizing high power switch is current distributed approach, the dissipated power also gets equally distributed across multiple devices and so is capable of handling CW power. And also, to test the device beyond 10W, to test the CW power survivability, a test bench is created with 25W CW GaN SSPA feeding the integrated T/R Switch with LNA. MMIC is packaged in metal ceramic package with CuW base and mounted on test jig with coaxial connectors. The photograph of the test bench is given in Fig. 7-4.

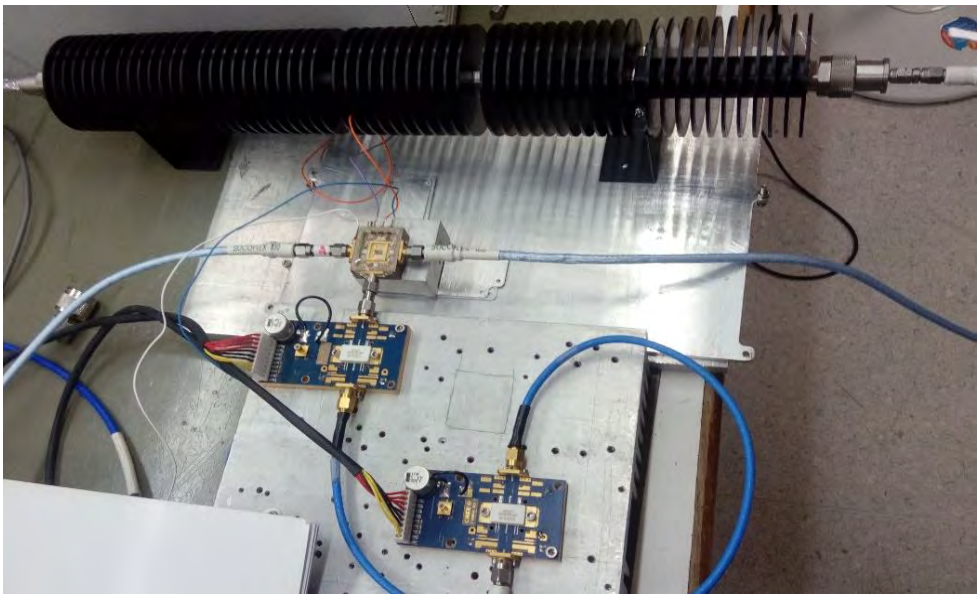


Figure 7-4. CW high power test for T/R Switch with LNA Test Bench

The CW power sweep test results are given in Fig 7-5. The switch insertion loss remains around 1.7 dB even at 20W CW power and 1.5 dB up to 14W, where the non-linearity sets in [9]. The interconnect losses of input and output connectors, link alumina substrates and interconnect 1 mil bond wires is around 0.5 dB which is not de-embedded from the measurement data. During the high power test, LNA was kept OFF and post high power test, the LNA performance is verified.

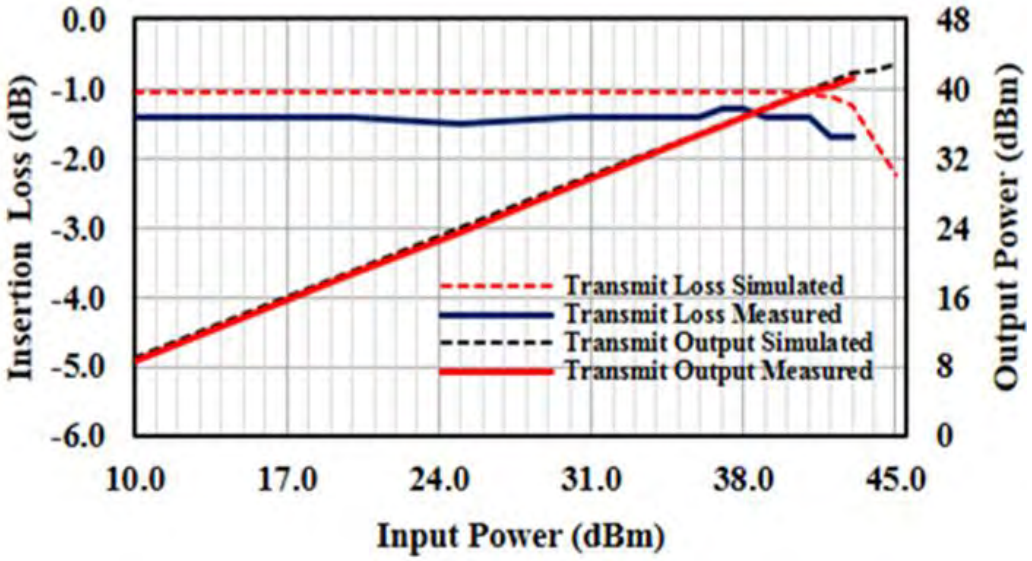
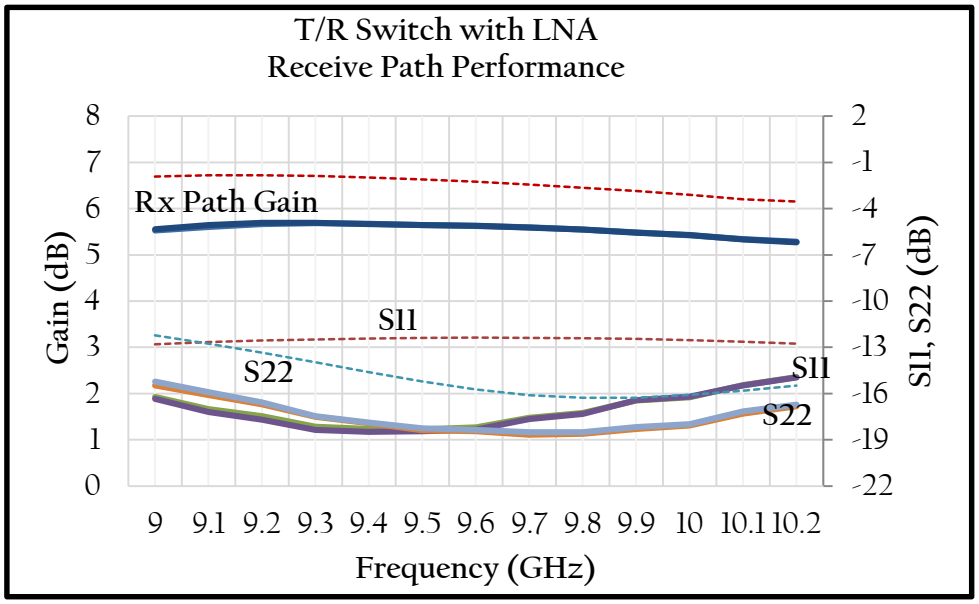


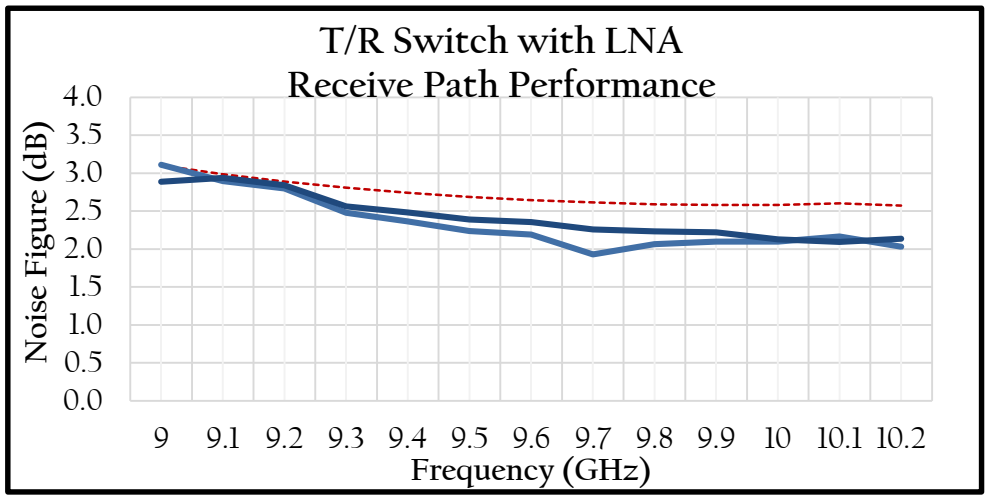
Figure 7-5. CW power sweep test results. Solid lines: measurement. Dashed lines: simulation

7.1.2.2 RF On-wafer test results of 10W T/R Switch with LNA

Two nos. of 10W T/R switch with LNA MMIC is on-wafer tested for all the S-parameters and the Noise Figure and the results are given in Fig. 7.6 (a) and (b).



(a)



(b)

Figure 7-6. On-Wafer Receive path performance of T/R switch with LNA (a) Input Return Loss, Output Return Loss & Receive Gain and (b) Noise Figure; Solid lines: measurement. Dashed lines: simulation

The spread is controlled and results follow the simulation trend with 0.5 dB improved Noise figure and 0.8 dB reduction in gain which can be attributed to the device model uncertainty. Higher power handling, more than the analyzed value, is because during the design conservative typical I_{DSS} of 350mA/mm was considered rather than the maximum I_{DSS} of 500mA/mm. Table 7-1 shows the performance comparison of 10W T/R switch with previously reported work.

Table 7-1

Comparison of performance of proposed 10W T/R switch with previously reported works

Ref.	Freq. (GHz)	Power Handling (W)	Tx path Loss (dB)	Rx Isolation (dB)	Rx Gain (dB)	Rx path Loss / NF (dB)
[7]	7-12	10	-	NA	14	2.7
[11]	30-38	5	-	NA	18	2.5
[3]	22-26	4	-	44	-	2.5
This Work	**9.3-9.9**	**17**	**1.0**	**28**	**6**	**2.5**

7.2 X-Band 20W absorptive Receive Protection Switch with integrated LNA

This high power Receive Protection switch with integrated LNA design is identical to Transmit/Receive Switch with LNA of the previous section, however, unlike in the previous design, in this receiver protection switch, the insertion loss in the receive path is traded off with the insertion loss in the high power path. In this work, T/R switch with integrated low noise amplifier is designed using 130nm psuedomorphic HEMT process, D01PHS of OMMIC foundry.

7.2.1 Design Approach and Schematic

The input 3-dB quadrature hybrid, on-the-chip coherent current distributed high power switch element in each of the arms of the hybrid, the single stage LNA and the output 3-dB quadrature hybrid are integrated to create 20W absorptive Receive protection switch with LNA. Already described and tested designs viz., compact spiral hybrid (section 4.2.3), high power switch element (section 5.3.1) and single stage LNA (section 6.4.2) are used for designing the 20W absorptive Receive Protection Switch with integrated LNA MMIC. Fig. 7-7 shows the schematic of 20W absorptive Receive Protection Switch with integrated LNA MMIC.

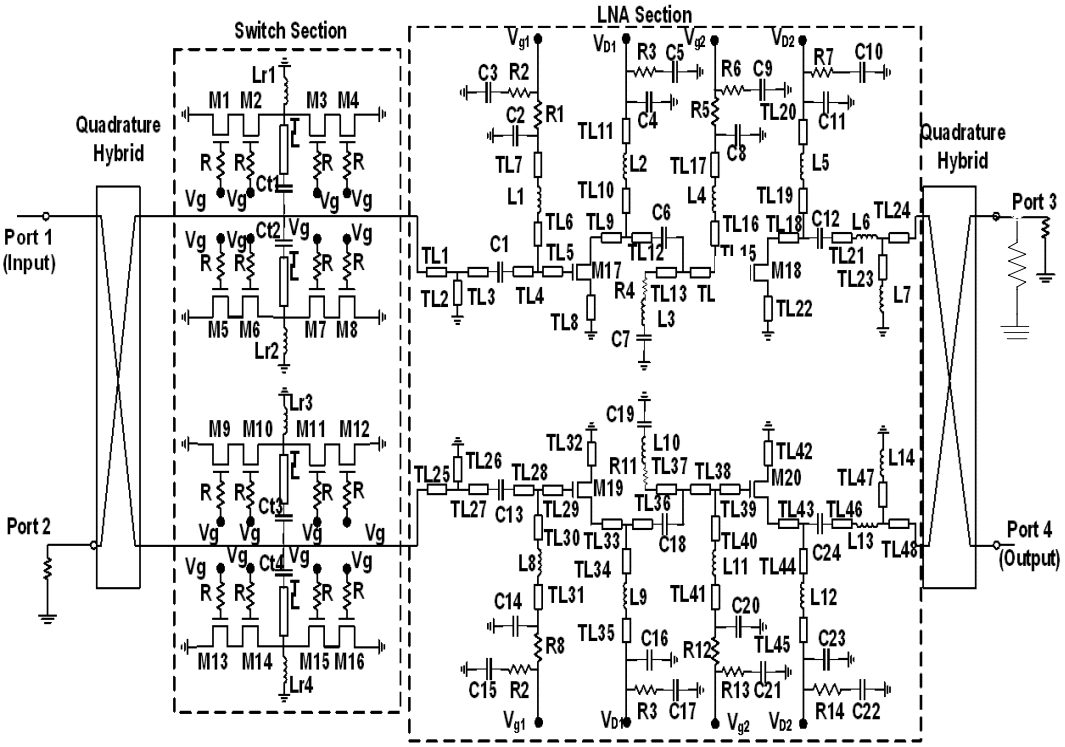
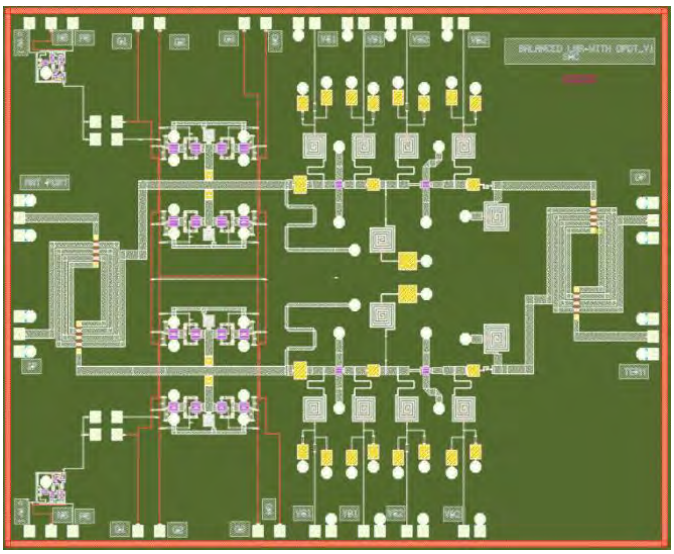
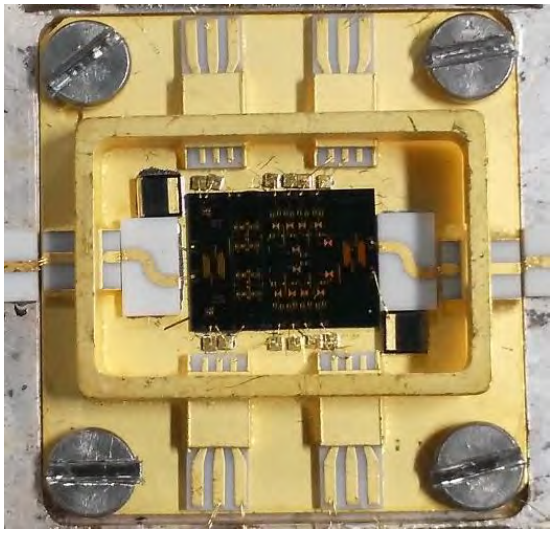


Figure 7-7. Schematic of 20W high power T/R Switch integrated with LNA

Complete structure is simulated for all the conditions, viz., transmit path loss and isolation assessment during power sweep and frequency sweep for Transmit operation mode and stability, receive path gain and noise figure over frequency sweep for Receive operation mode, using linear and harmonic balance analysis in CAD tool, ADS, with linear and non-linear cold FET device model from the foundry. Fig. 7.8 (a) and (b) show the layout of realized MMIC and photograph of the assembled MMIC in metal ceramic package.



(a)

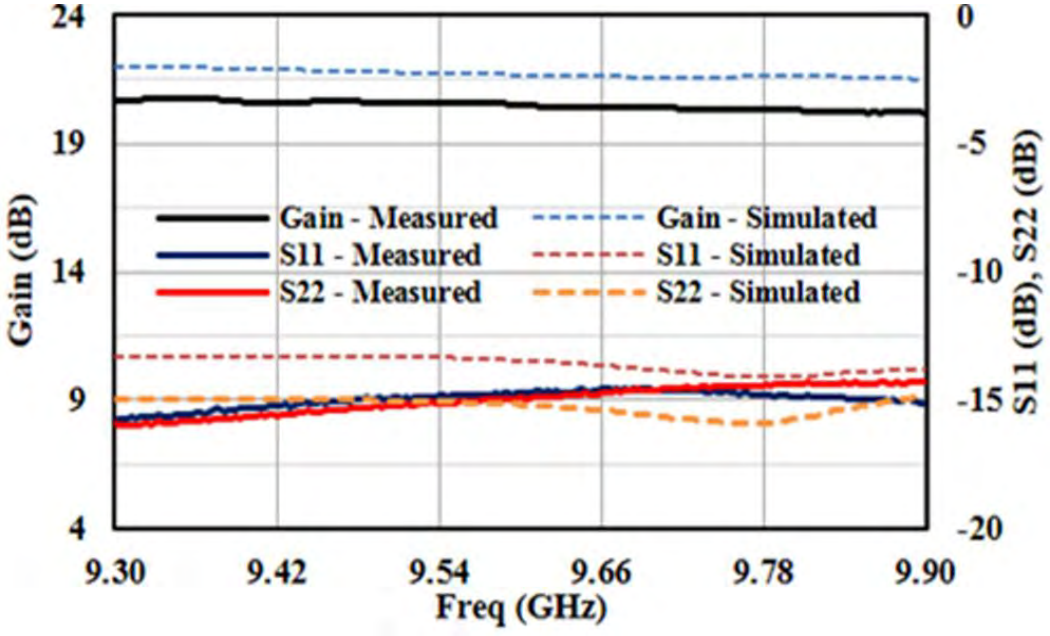


(b)

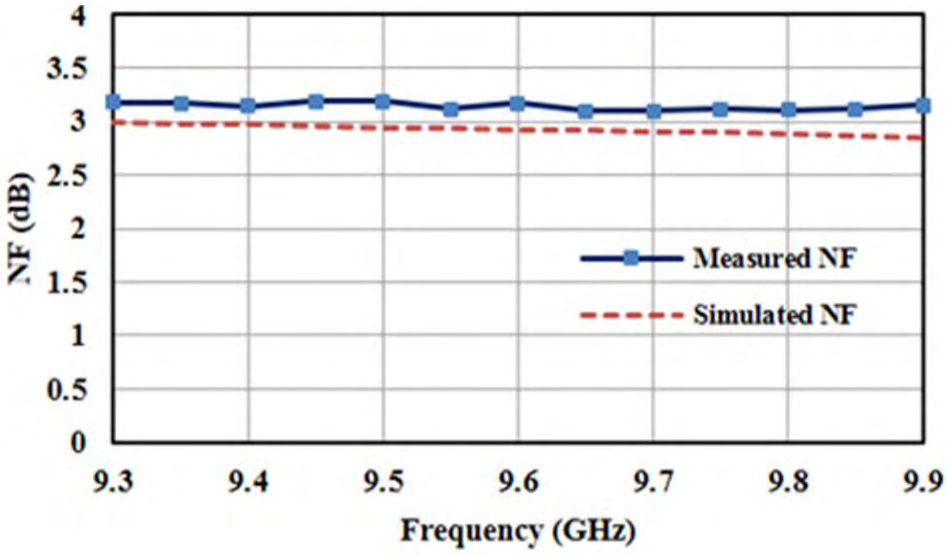
Figure 7-8. (a) MMIC layout of Current paralleled, Stacked FETs Receive Protection Switch with integrated 2-stage LNA and (b) Photograph of realized MMIC assembled in metal-ceramic package.

7.2.2 Measurement Results

The 20 W receive protection switch with LNA MMIC, from the initial prototype fabrication run, is bonded in a metal-ceramic package and assembled on a test jig with coaxial connectors on the input and output ports, as shown in Fig. 7.8(b). Figure 7.9 (a) shows gain, input and output return losses and figure 7.9 (b) shows the NF of the device in receive mode.



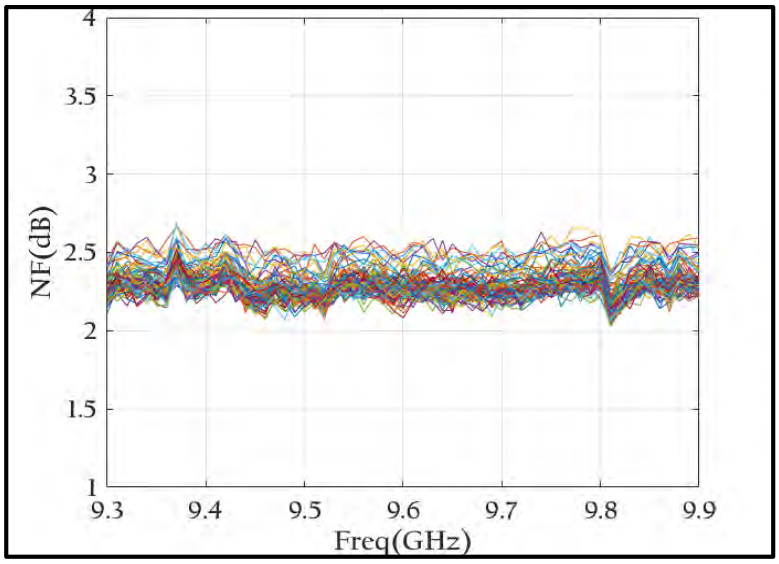
(a)



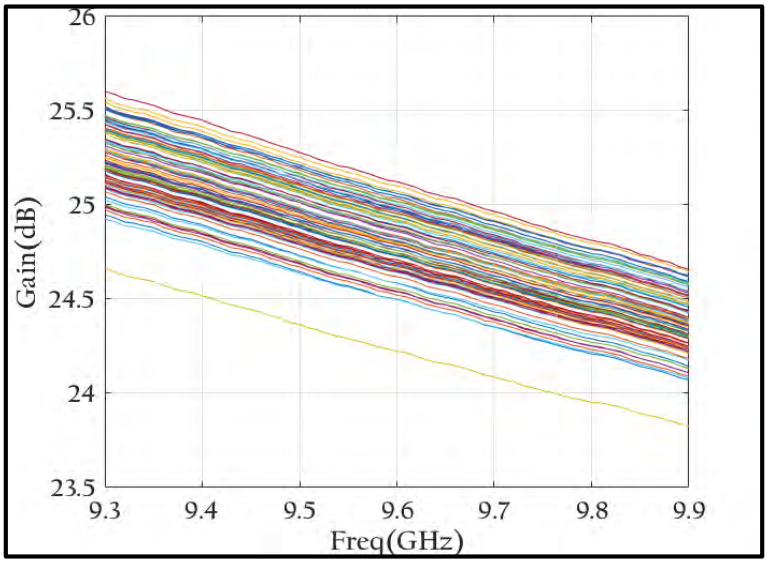
(b)

Figure7-9. Test result of 20W Receive protection switch with LNA. (a) Gain and Return Losses (b) NF

Subsequently, during the production run, one complete 3-inch wafer containing only the 20 W receive protection switch with LNA MMIC is fabricated. Fig. 7-10 (a) shows the on-wafer measurement result of noise figure in receive mode. Noise figure is better than 2.6 dB over 85 numbers of die fabricated on a 3-inch wafer. Fig. 7-10 (b) shows the variation in gain among 85 numbers of fabricated die. Nominal gain varies from 25.25 dB to 24.25dB and variation of gain among fabricated die is less than 1dB.



(a)



(b)

Figure7-10. RF on-wafer measurement of T/R switch integrated with LNA: (a) Noise figure in Receive mode. (b) Gain in receive mode

The controlled performance spread across 85 Nos. of MMICs, in a given wafer, shows excellent design centering, validating the design. The CW power handling capability of the switch has already been tested and presented in section 5.4.3.

Table 7-2

Comparison of performance of proposed 20W absorptive Receive Protection MMIC with previously reported works

Ref.	Freq. (GHz)	Power Handling (W)	Receive Isolation (dB)	Receive Gain (dB)	Receive path Loss / NF (dB)
[4]	8-10	10	25	-	2.0
[7]	7-12	10	NA	14	2.7
[11]	28-38	2	NA	21	2.3
[11]	30-38	5	NA	18	2.5
[3]	22-26	4	44	-	2.5
This Work	**9.3-9.9**	**>20**	**28**	**20**	**<2.9**

7.3 S-band GaN 200W T/R Switch with integrated LNA

As GaN power process is also suitable for realizing LNAs, the on-the-chip coherent current distribution technique is employed for designing S-band 200W T/R switch with LNA using 0.25µm GaN pHEMT process from UMS (GH25-10), which has typical parameters like Vp=-3.5V, V_{DS} max=90V @ V_{GS}=-20V, I_{DSS} typ.=825mA/mm.

7.3.1 Design Approach

Following the design approach detailed in section 3.2.3, i.e., *impedance transformation along with on-the-chip current distribution technique*, the input 3-dB impedance transforming quadrature hybrid, on-the-chip coherent current distributed high power switch element in each of the arms of the hybrid, the GaN LNA and the output 3-dB non-impedance transforming quadrature hybrid are integrated to create a GaN 200W T/R switch with LNA.

The already described and optimized designs viz., compact spiral hybrid (section 4.3), high power switch element (section 5.4.1) and GaN LNA (section 6.5) are used for designing the GaN 200W T/R switch with LNA MMIC. Fig. 7-11 shows the schematic of 200W T/R switch with LNA MMIC.

7.3.2 Integrated 200W T/R Switch with LNA

The impedance transforming input hybrid, high power switch element, additional switch stage for isolation, matching network, two-stage LNA and non-transforming output hybrid are integrated. Fig. 7-11 and 7-12 shows the schematic and layout of the MMIC.

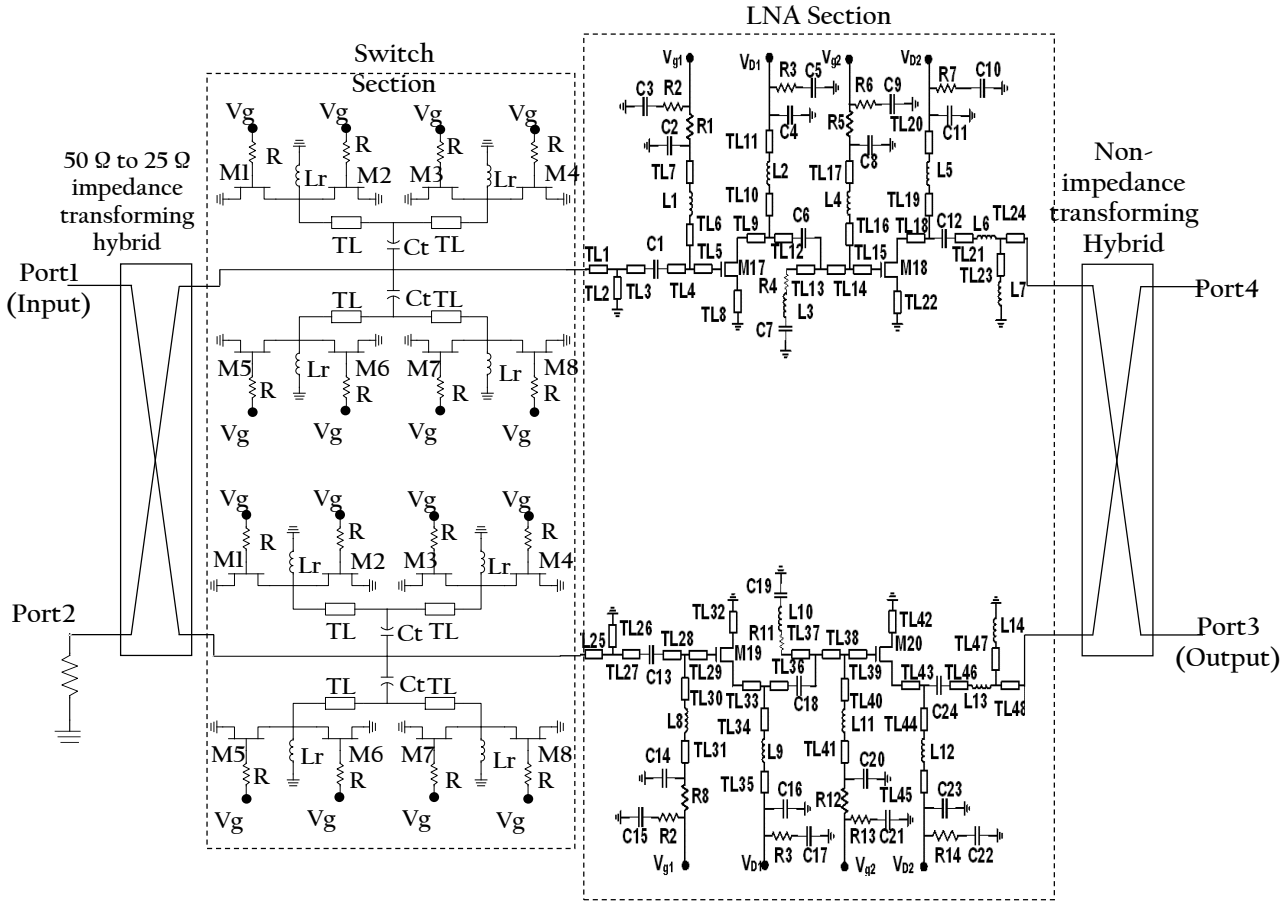


Figure 7-11. Schematic of 200 W T/R Switch with integrated LNA

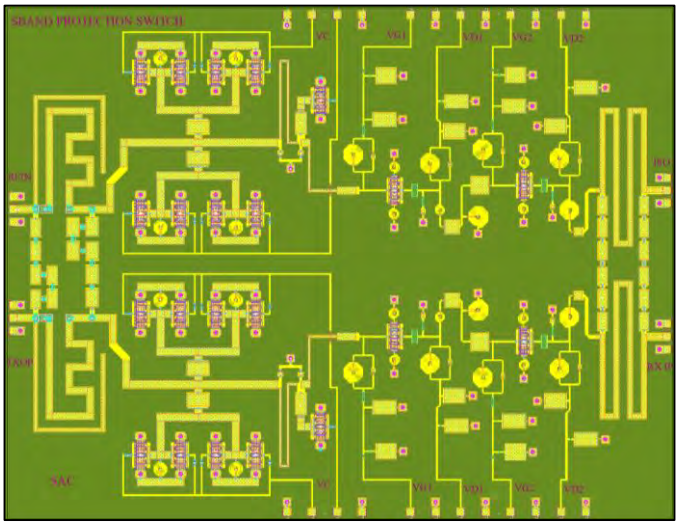


Figure 7-12. Layout of 200 W T/R Switch with integrated LNA

7.3.3 Simulation Results of 200W T/R Switch with LNA

Electromagnetic simulation of 200W receive protection switch with LNA MMIC layout is carried out using ADS. Non-linear FET model is used in co-simulation to analyse the performance of the switch with LNA. Fig. 7-13 shows the simulated results of receive path of T/R switch. Fig. 7-14 shows the simulated results of T/R switch in transmit mode.

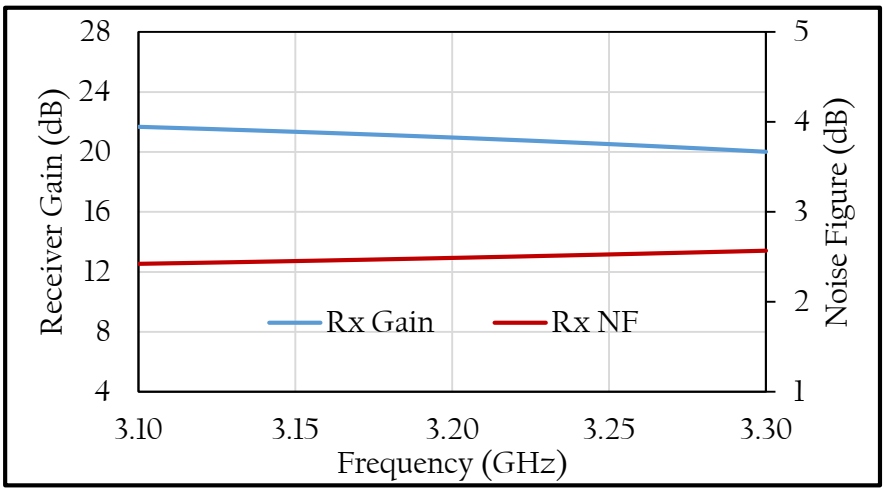


Figure 7-13. Simulated results of 200W T/R switch in Receive mode

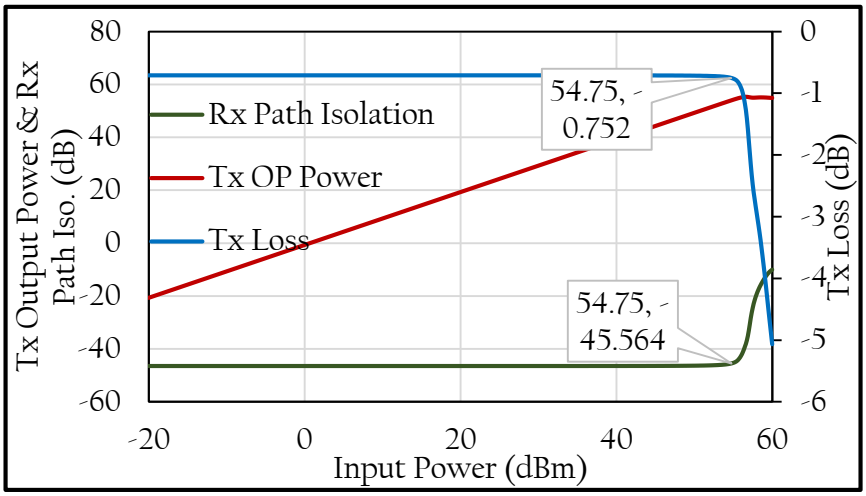


Figure 7-14. Simulated results of 200W T/R switch in Transmit mode

Simulated NF varies from 2.4 to 2.57 dB and gain varies from 21.8 to 20.5 dB across the band. Simulated input and output return loss are better than 15dB across the operating bandwidth. Transmit loss and receive isolation are better than 0.75dB and 38dB respectively. Table 7-3 shows the comparison of proposed 200 W T/R switch with LNA with previously reported works.

Table7-3

Comparison of performance of proposed 200 W T/R switch with LNA with previously reported works

Ref.	Freq. (GHz)	Power Handling (W)	Tx path Loss (dB)	Rx Isolation (dB)	Rx Gain (dB)	Rx path Loss / NF (dB)
[13]*	5.25-5.57	40	-	-	36	2.5
[14]*	5.7-6.7	2.5	-	-	8	3.7
[15]*	5.2-5.6	63	0.5	45	31.5	2.4
[17]*	7.7-12.2	20	0.8	-	14	3.0
[18]*	8.6-11.2	8	-	-	15.5	2.75
[19]*	S-band	75	0.5	>30	30	1.75
This Work**	**3.1-3.3**	**200**	**<1.0**	**>45**	**>20**	**<2.6**

*GaN Single Chip Front-ends with T/R Switch and LNA
** design and layout level simulation

7.4 Conclusions

- ✓ Employing **novel impedance transformation technique along with on-the-chip coherent current distribution**, 200W S-band GaN T/R switch with LNA has been designed, analyzed and layout level electromagnetic and co-simulation results are presented.
- ✓ Employing **novel on-the-chip coherent current distribution technique**, 10W X-band GaAs T/R switch with LNA, employing low power foundry process, has been designed, analyzed, simulated, fabricated and tested at both on-wafer and assembled stages.
- ✓ Employing **novel FET stacking** along with **on-the-chip coherent current distribution technique**, 20W X-band GaAs Receive protection switch with LNA, employing low power foundry process, has been designed, analyzed, simulated, fabricated and tested at both on-wafer and assembled stages.
- ✓ **Performance comparison carried out with the published works and the present work presents highest power handling capability T/R Switch / Receive Protection switch with integrated LNA, employing low power GaAs process.**

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Chapter: 8

Conclusions & Future Scope of Work

Conclusions:

The conventional high power microwave signal switching component is the Silicon/GaAs PIN diode, while the recently GaN pHEMT devices are being used for this application. When a GaAs FET is used as a switching element as a PIN diode replacement in several applications, it has the advantages of having fast switching speeds, simplified bias networks, monolithic compatibility, and lower power consumption driver circuitry. The major advantage of having a GaAs FET based high power T/R Switch or protection switch is that, other functionalities of Receiver can be integrated on to MMIC (Monolithic Microwave Integrated Circuit) making a multi-functional core-chip. However, the power performance of a FET is limited by its current-handling capability in its low-impedance state and by its breakdown voltage in its high-impedance state.

In this thesis, various novel circuit architectures are presented for increasing the power handling capability of GaAs FET based switches, *using low noise and low power processes*, to enable the realization of high power T/R switch with integrated LNA or absorptive high power receive protection switch with integrated LNA. Similar technique is employed on GaN FET based switches to further increase the power handling capability beyond that of individual GaN FET switch, and also integrating LNA using the same GaN process. The constituent components required for designing T/R Switch with LNA, viz., high power quadrature hybrids, high power switches, LNAs are studied and design details are presented.

Various high power MMIC quadrature hybrid configurations have been studied and the design, analysis and simulation results of compact distributed *high power MMIC spiral hybrid* and "modified" *high power MMIC quasi lumped impedance transforming hybrid* are presented.

MMIC GaAs and GaN HEMT based switch configurations have been studied vis-a-vis the power handling capability and novel techniques like *on-the-chip current distributed architecture* for increasing the power handling capability and *techniques of*

impedance transformation and FET stacking techniques for improving the insertion loss are proposed, analyzed and simulation results are presented.

MMIC GaAs HEMT based Low Noise Amplifiers' configurations have been studied and X-band single stage and two-stage LNA design, simulations and measurement results are presented. MMIC GaN HEMT based S-band Low Noise Amplifier design and simulation results are presented.

On-the-chip current distributed architecture, for increasing the power handling capability, is proposed, analyzed and employed for realizing a **GaAs MMIC 10W T/R switch with integrated LNA**, employing 0.25-µm GaAs pHEMT process (PH25 of M/s UMS, France). The measured transmit loss, Noise Figure (NF) and receive path gain are 1.0 dB, 2.5 dB and 5.6 dB respectively, over 9.3-9.9 GHz.

Novel *impedance transformation along with on-the-chip current distribution technique*, for increasing the power handling capability and improving the receive path loss, is proposed, analyzed, and employed for designing a **GaN MMIC 200W T/R switch with integrated LNA**, using 0.25-µm GaN pHEMT process (GH25 of M/s UMS, France). The layout level electromagnetic and co-simulation results of this 200W pulsed power handling capability T/R switch with integrated LNA are 45 dB isolation, 2.6 dB NF and 20 dB gain over 3.1-3.3 GHz. *The control voltage needed for this switch operation is +2/-4V only, in comparison to conventional +2/-30V while employed as OFF FET.*

Also, in this thesis, novel *FET stacking along with on-the-chip current distributed architecture,* for increasing the power handling capability and improving the receive path loss, is proposed, analyzed and employed for realizing a **GaAs MMIC 20W absorptive Receive protection switch with integrated LNA**, employing 0.13-µm GaAs pHEMT process (D01PHS of M/s OMMIC, France). The measured results are protection up to 20W, 2.9 dB NF and gain of 20 dB over 9.3-9.9 GHz.

Novel techniques for increasing the power handling capability of FETs, GaAs or GaN, beyond individual device ratings, along with RF performance trade-offs are presented and validated with experimental data.

This is a scalable architecture, implementable using the standard Process Design Kit (PDK) offered by foundries. To the best of author's knowledge, the present work demonstrates highest power handling capability T/R switches and absorptive Receive protection switches with integrated LNA, using low power GaAs processes.

Future Scope of Work:

- Novel techniques for increasing the power handling capability of FETs, GaAs or GaN, beyond individual device ratings, along with RF performance trade-offs are presented and validated with experimental data. These techniques can be combined with already in vogue techniques like *distributed architecture* for increasing switch power handling capability, isolation and Limiter designs.

- Proposed techniques are scalable architecture, implementable using the standard Process Design Kit (PDK) offered by foundries and hence useful for realizing high power T/R switches/protection switches using single process, which aids in realizing different RF functionalities on a single MMIC.

- Presently, limited work is reported on FET based high power Limiters. The present architecture proposed is ideally suitable for realizing **"FET based absorptive high power Limiters".**

- Schottky based Limiters or FET based high power Limiters, do not have "Flat Leakage" characteristic, unlike PIN diode based Limiters, owing to fast recovery time of Schottky junctions. The present architecture and design can be modified and can be made to realize **"FET based absorptive high power Limiters with Flat Leakage",** by controlled exploitation of Gate-drain coupling in a distributed architecture.

Papers Published / Presented

- Ch V N Rao, D K Ghodgaonkar, Nitesh Sharma, "GaAs MMIC Low Noise Amplifier With Integrated High-Power Absorptive Receive Protection Switch" – **IEEE Microwave and Wireless Components Letters, vol. 28, no. 12, pp 1128-1130, Dec. 2018.**

- Ch V N Rao, D K Ghodgaonkar, Piyush Sinha, Rajeev Jyoti, "MMIC High Power Transmit/Receive Switches with integrated Low Noise Amplifiers using GaAs and GaN Processes" –**IEEE MTT-S International Microwave and RF Conference (IMARC), Kolkata, India, Nov. 2018.**