Comparative study of performance parameter of Phase-Locked Loops in CNTFET and CMOS technologies at deep sub-micron level

by

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Declaration

I hereby declare that

(i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

(ii) due acknowledgement has been made in the text to all the reference material used.

Signature of Student

Certificate

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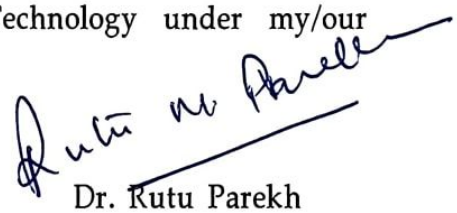

Dr. Rutu Parekh
Thesis Supervisor

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Abstract

We discuss about the improving performance of PLL using CNTFETs with circuit architecture along with its simulation results. There is no such work presented before which illustrate the complete PLL design using CNTFET. The schematic of simulation circuit is based on conventional design of Phase-Locked Loop. The model used is virtual-source CNTFET model which describes enhancement mode, unipolar MOS transistors with semiconducting single walled CNT as channels. The model is based on a quasi-ballistic transport and embraces a precise explanation of the capacitor network in a CNTFET. All the circuit design and simulation performed in Cadence Virtuoso and general idea of layout taken from different references to get an approximate idea of area occupied by the PLL. As compared to PLL using MOSFET at 45nm, 16nm CNTFET based PLL gives approximately upto 33% more frequency signal at output, and consumes upto 90% less power and area.

List of Principal Symbols and Acronyms

ω	Frequency
$d\varphi$	Differential change in phase
dt	Differential change in time
$v_e(t)$	Error Voltage
K_{PFD}	Gain of PFD
$\varphi out(t)$	Phase of Output Pulse
$\varphi in(t)$	Phase of Input Pulse
ω_{out}	VCO output frequency
ω_0	VCO frequency at zero control voltage
K_{VCO}	Gain Sensitivity of VCO
V	Voltage
I	Current
B.W.	Bandwidth
Vdd	Power Supply Rail
R	Resistor
C	Capacitor

Other minor symbols are defined at first occurrence; where necessary some symbols are redefined in the text.

PLL	Phase-Lock Loop
PFD	Phase-Frequency Detector
CP	Charge-Pump
LPF	Low-Pass Filter
VCO	Voltage-Controlled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
CNTFET	Carbon-Nanotube Field Effect Transistor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
Si	Silicon
CLK_{REF}/ref	Reference Clock/Reference signal
CLK_{FB}/vco	Feedback Clock/Feedback vco signal
D-FF	Delay-Flip Flop
V_{ctrl}	Control Voltage
type	type of transistor. 1: n-CNTFET; -1: p-CNTFET
s	spacing between the CNT
W	transistor width
L_g	physical gate length
L_C	contact length
L_{ext}	source/drain extension length
d	CNT diameter
t_{ox}	gate oxide thickness
k_{ox}	gate oxide dielectric constant

k_{cnt}	CNT dielectric constant
k_{sub}	substrate dielectric constant
k_{spa}	source/drain spacer dielectric constant
H_g	Gate height
E_{fsd}	Fermi level to the band edge [eV] at the source/drain.
V_{fb}	Flat band voltage (for threshold voltage adjustment)
Geomod	Device geometry 1: cylindrical gate-all-around 2: top-gate with charge screening effect 3: top-gate without charge screening effect
Rcmod	Contact mode 0: user-defined value, Rs0 1: diameter-dependent transmission line model 2: diameter-independent transmission line model
Rs0	User-defined series resistance
SDTmod	Source-to-drain tunnelling 0: SDT inactivated 1: SDT with inter-band tunnelling 2: SDT without inter-band tunnelling
BTBTmod	band-to-band tunnelling mode: 0-off, 1-on
temp	temperature (°C)
DIBL	Drain-Induced Barrier Lowering
S	Source
D	Drain
G	Gate
V_{ds}	Drain-to-Source Voltage
V_{gs}	Gate-to-Source Voltage
V_{TH}	Threshold Voltage

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Chapter 1
Introduction

1.1 General

A phase-locked loop or PLL is a closed loop feedback circuit comprises of four key components phase frequency detector, charge pump, low pass filter and voltage-controlled oscillator. These blocks are connected to form a closed loop feedback network so as to synchronize the output with the input in both phase and frequency [1]. And this loop continues to run until PLL locked condition is achieved i.e., either zero or constant phase difference between the reference input and the feedback pulse from the output of PLL. PLL is castoff as frequency synthesizer, on chip clock generator and clock and data retrieval system computers and telecommunication system. In general, as technology scale down a PLL with widespread tuning range, high operating frequencies and low jitter are preferred [2].

In this paper, a comparative analysis is made between the performance parameters of PLL in CMOS and CNTFET technologies. Single-walled CNTFETs have been among the primary contenders to match Silicon CMOS and encompass CMOS technology scaling in the deep sub-micron's technology nodes. In Si-MOSFET device one of the foremost factors obstructing more scaling is the short-channel effects, which causes MOSFETs at short gate lengths to be grim to turn OFF, subsequently consuming much power [3, 4]. A paper by Sinha et al., [5] alleged that as compared to MOSFET, CNTFETs have higher channel mobility and better gate capacitance against gate voltage also CNTFET gate capacitance decreases with a reduction in oxide thickness at the nanometre scale. This reduction can be detected at a gate voltage of 0.5V and above which tends to decrease propagation delay and leakage current in comparison to MOSFET [6]. Also, the consequence of an increase in temperature on the threshold voltage of CNT transistors is very trivial as compared to MOSFET [7].

1.2 Organisation of the Thesis

As mentioned, section 1.1 of chapter 1 gives a basic introductory idea on PLL and CNTFETs in comparison with MOSFETs technology. From chapter 2 onwards of the critique include designing each block of PLL including a frequency multiplier for increasing the range of output frequency. Subsequently, chapter 3 shows the modelling of cast-off CNTFET and the parameter of CNTFET used while simulation followed by chapter 4 which shows the simulation (mainly includes transient analysis) of complete PLL and Frequency Multiplier followed by the simulation result of some of the performance matrices like dead zone and temperature analysis. This section also shows the comparative study of this work with others.

Chapter 2
Design of Phase-Locked Loop

PLL has been extensively used in FM demodulation, AM demodulation, control system applications, and wireless communications. The main area of application of PLL are clock recovery, inter-chip communications, and frequency synthesis and it can also be used to reduce jitter in the clock signal. As clock accuracy always being a vital parameter, many systems have been using frequency synthesizers to deliver several clocks to their circuits [8]. Nowadays PLL is the key component of all SOCs since it is the only circuit that generates the high-frequency clock signal. It is a closed-loop control system that senses the phase error in the output waveform by comparing it with the input waveform and the loop continues till we get a constant or zero phases difference between both the waveforms/signals. Fig. 1 shows the elementary block diagrammatic representation of the Phase-Locked Loop (PLL) which consists of a Phase-Frequency Detector (PFD), Charge Pump (CP), Low-Pass Filter (LPF), and Voltage-Controlled Oscillator (VCO).

The phase error is sensed by the PFD block where one input to the PFD block is the reference waveform i.e., CLK_{REF} and another waveform is the feedback from the output of VCO i.e., CLK_{FB} whereas f_{Out} is the output frequency of PLL which is fed to the external circuitry. A query might rise that clock signal can be generated from stable reference oscillator then what is the necessity for PLL. This can be defensible as the stable reference oscillator which generates the clock signal has low-frequency output so to produce the high-frequency clock signal, we need VCO [9].

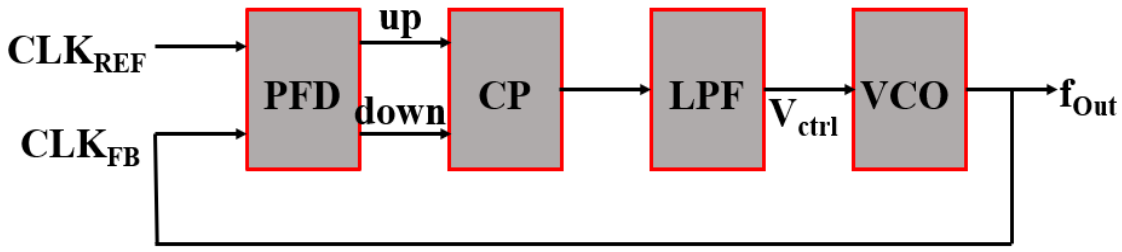


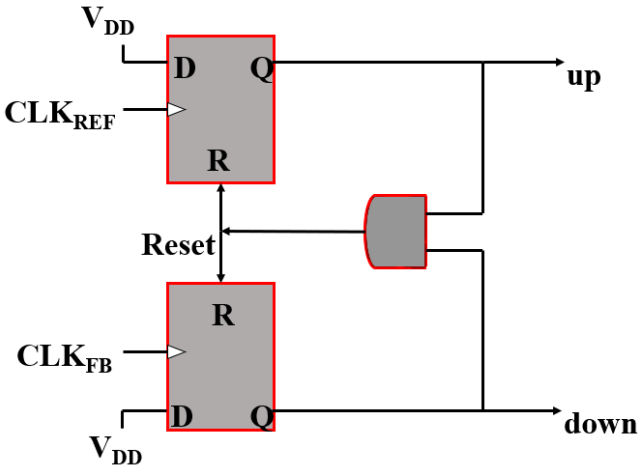
Figure 2.1 Basic block diagram of PLL

2.1 Phase-Frequency Detector

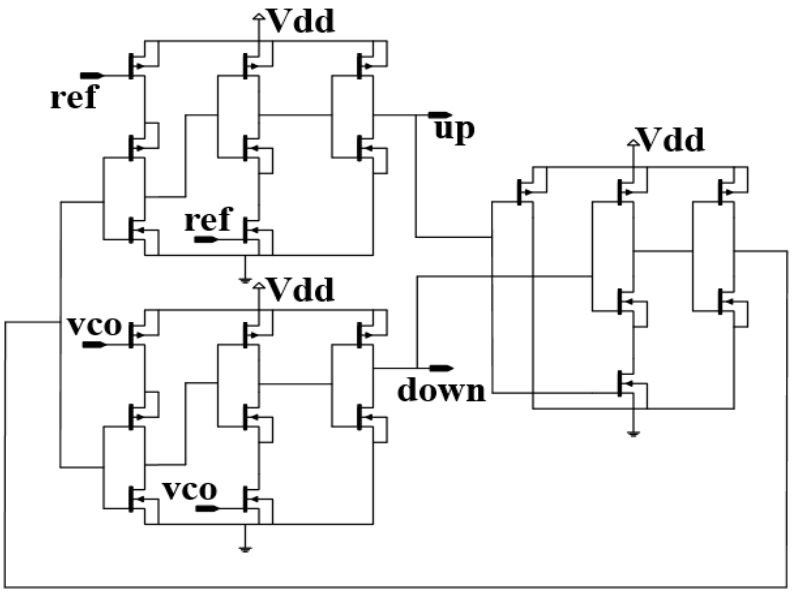
The concept behind PFD is it compares the two-input signal and produces an error signal proportional to the difference between the two input waveforms so for PLL it is used as an error-detecting block. Fig. 2 represents the PFD, it uses two D-FFs whose input is kept always at high potential, and the reference signal is provided at the clock input of one of the D-FFs i.e., CLK_{REF} and the output of VCO is feedback to the clock input of another D-FF i.e., CLK_{FB}.

An AND gate is provided at the output of both D-FFs to generate a reset signal and set the output of both the D-FFs to zero whenever both the signal “up” and “down” is high. The "up" signal is produced when the rising edge of CLK_{REF} is leading the rising edge of CLK_{FB} and the “down” signal is generated when the rising edge of CLK_{FB} is leading the rising edge of CLK_{REF}. When the up signal is generated (high) as shown in Fig. 3(a), this signifies that the reference signal is leading the VCO output so to match the reference waveform and feedback waveform VCO input must be tuned such that it generates a high-frequency output signal. This process continues till both the signal matches and PLL enters into lock condition.

Similarly, when the down signal is generated (high) as shown in Fig. 3(b), this signifies that VCO output leads to the reference signal so VCO must be tuned such that it generates a low output frequency till it matches with the reference signal [10].



(a)



(b)

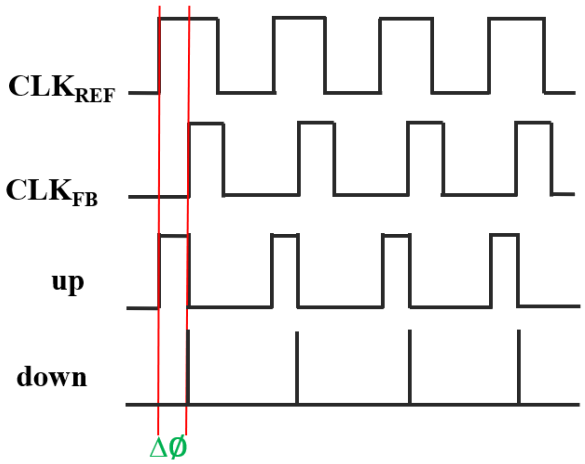
Figure 2.1.1 Design of PFD (a) Phase-Frequency Detector (b) PFD at the transistor level

The corresponding pulse width of the "up" and "down" signal in Fig. 3(a) and Fig. 3(b) respectively is directly proportional to the phase alteration between the reference input and VCO output. Now when both the input of D-FFs becomes high then "up" and "down" become zero because of AND gate which provides a reset signal to both the D-FFs. So, PFD can only operate in three states and is hence also termed a 3-state phase detector.

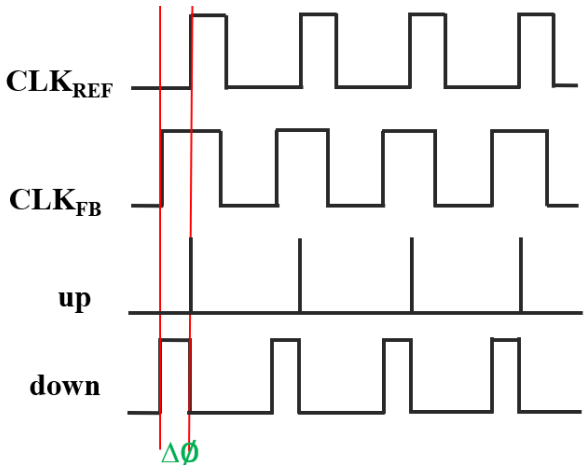
The phase and frequency interrelation are shown in Eq. 1.

$$\omega = \frac{d\varphi}{dt} \tag{1}$$

And Eq. 2 shows the error signal i.e., $v_e(t)$ directly proportional to the phase alteration between the two input waveforms.



(a)



(b)

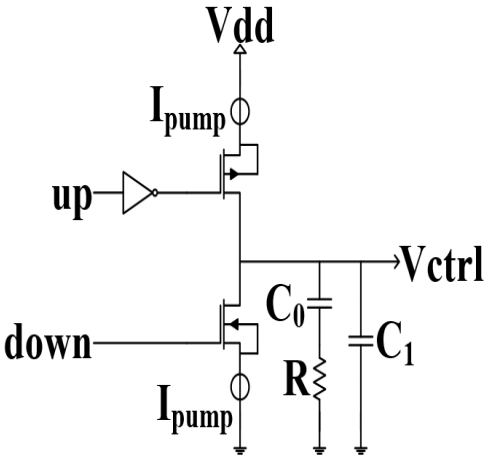
Figure 2.1.2 Reference PFD output waveform (a) Reference signal leads Feedback Signal (b) Reference signal lags Feedback Signal

K_{PFD} is the gain of the phase detector (V/rad).

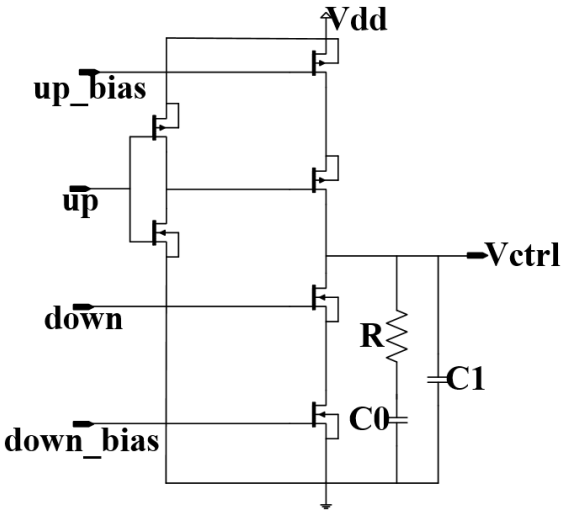
$$v_e(t) = K_{PFD} * [\varphi out(t) - \varphi in(t)] \quad (2)$$

2.2 Charge-Pump and Low-Pass Filter

Charge pump-based PLL has been extensively castoff in various high-speed designs, like microprocessors or communication systems. A charge pump is a bipolar switch that is controlled by the three states of the PFD. As shown in Fig. 4, the Conventional charge pump has two symmetrical current sources and two transistors that act as a switch. It generates both the polarity of current pulses into LPF. LPF is used in PLL to get rid of the high-frequency components in the output of the PFD. It also removes the high-frequency noise. Sometimes an amplifier is also used with LPF to obtain gain at the output. The polarity of output current from the charge pump depends upon which of the "up" or "down" signal is high (logic 1), and this state is established by the sign of phase error through PFD [11, 12].



(a)



(b)

Figure 2.2 Design of CP (a) Conventional charge pump with LPF (b) CP at the transistor level

As a rule of thumb, the capacitances in LPF are C1 and C0 given by $C1 = \frac{C0}{10}$. And the corresponding bandwidth of the filter is given by Eq. 3.

$$B.W. = \frac{1}{(1+RC)} \quad \text{and C is given by, } C = \frac{C0*C1}{(C0+C1)} \tag{3}$$

Table I shows the operation of the charge pump circuit.

TABLE I
CHARGE PUMP OPERATION

Up	Down	Operation	Description
0	1	Discharging of a circuit node	Current streams out from the filter and discharges LPF capacitor
1	0	Charging of circuit node	Current streams into the filter and charges LPF capacitor
0	0	Constant output voltage	Zero Current

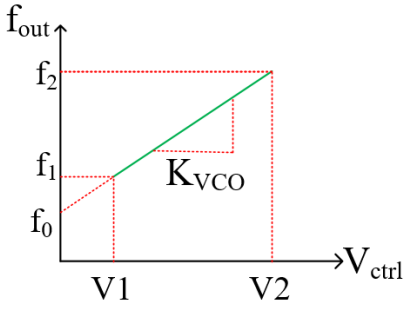
2.3 Voltage-Controlled Oscillator

VCO is the utmost vital block in PLL. It produces a high-frequency output signal in phase with reference input waveform to PLL. In an ideal VCO, there is a linear relationship between "f_{out}" i.e., output frequency, and "Vctrl" i.e., control voltage as shown in Fig. 4. This implies that the oscillation frequency of VCO can be varied by the varying input control voltage.

$$\omega_{out} = \omega_0 + K_{VCO} * Vctrl \tag{4}$$

Here, ω_0 represents the intercept at $Vctrl = 0$ and K_{VCO} denotes the sensitivity or gain of the circuit (in rad/s/V). The attainable range, $\omega 2$ - $\omega 1$, is called the tuning range.

(a)



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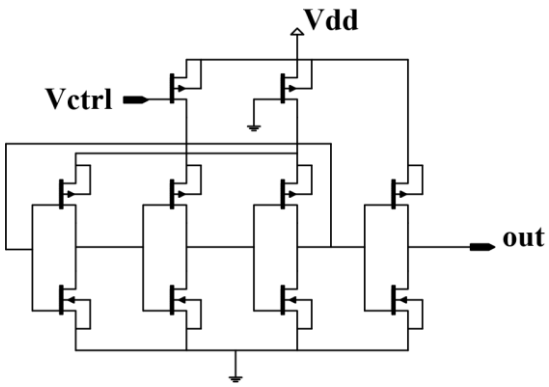
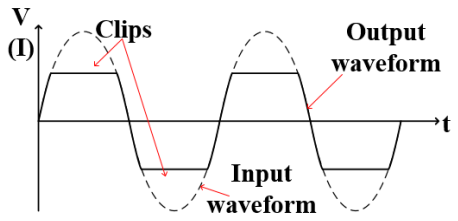


(c)

Figure 2.3 Design of VCO (a) VCO block diagram (b) Output frequency vs control voltage characteristics of VCO [13] (c) VCO at transistor level

2.4 Frequency Multiplier

It is a circuit that produces a signal whose frequency is a multiple of its input waveform. It consists of a non-linear combiner circuit that alters the input waveform and accordingly produces harmonics of the input waveform trailed by a filter that picks the wanted harmonic frequency and eliminates the unwanted fundamental and other harmonics components from the output. Frequency multipliers are often used in communications circuits and frequency synthesizers. In a journal by Zheng et al., [14] proposed a method known as the third harmonic enhancement technique to make a broadband and low-phase-noise CMOS frequency tripler. The concept of the third harmonic enhancement technique is to make a "deep cut" into each half of a given waveform, rather than a “clip” at each peak as conventional overdriven technique, the output signal potentially more resembles a triple frequency waveform rather than the square wave as shown in Fig. 6(b).



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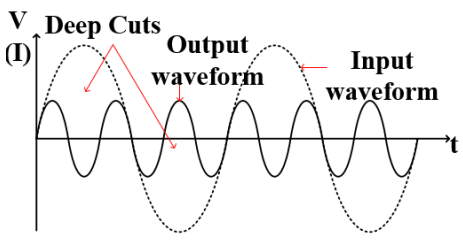

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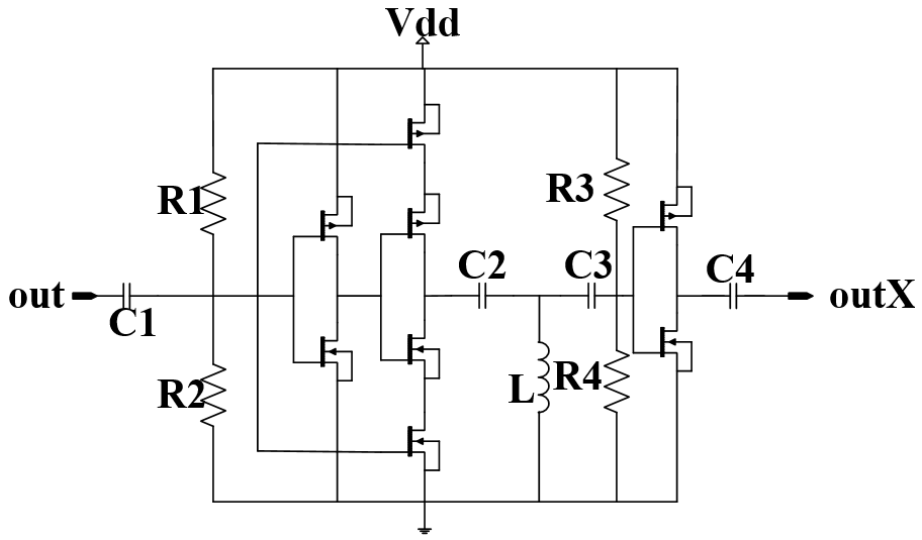


(c)

Figure 2.4 Design of Frequency Multiplier (a) Overdriven techniques with clip (b) With third harmonic enhanced technique with deep-cuts (c) Frequency Multiplier at the transistor level

Chapter 3
Cast-Off CNTFET Model and Simulation Setup

A paper, by Lee et al., [3, 4] shows that in Si-MOSFET devices one of the primary aspects hindering further scaling is the short-channel effects like Impact Ionization, drain-induced barrier lowering (DIBL), Hot Carrier Injection, Velocity Saturation, and Surface Scattering, so to overwhelmed these effects single-walled CNTFETs have been among the first choice. Also, in another paper by Sinha et al., [15] they have determined that in the deep sub-micron technology, CNTFET devices are gainful over double gate MOSFET due to lesser quantum capacitance, while in double-gate MOS transistors the magnitude of quantum capacitance goes on increasing which results in performance degradation by the increase in propagation delay.

The model used in this paper is the Stanford Virtual-Source Carbon Nanotube Field-Effect Transistors (VS-CNTFET) model shown in Fig. 6, which is a semi-empirical model that defines the I-V characteristics in a short-channel MOS transistor with CNT as the channel material [16].

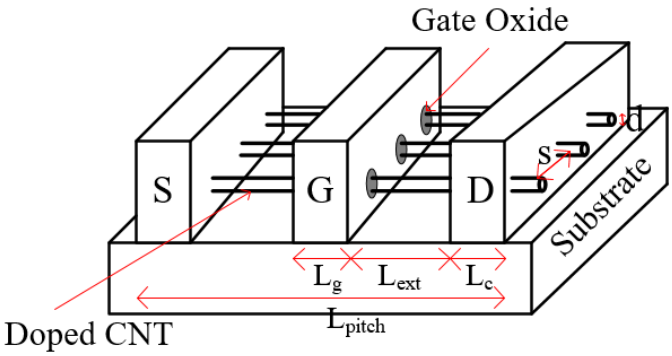


Figure 3.1 VS-CNTFET Model [3, 4]

TABLE II
CNTFET PARAMETERS

		CNTFET	
Input	**Value**	**n-type**	**p-type**
type	1	1	-1
s	10 nm	1 um	1 um
W	1 µm	20 nm	40 nm
L_g	11.7 nm	16 nm	16 nm
L_c	12.9 nm	11 nm	11 nm
L_{ext}	3.2 nm	3 nm	3 nm
d	1.2 nm	1.2 nm	1.2 nm
t_{ox}	3 nm	3 nm	3 nm
k_{ox}	23	3	23
k_{cnt}	1	1	1
k_{sub}	3.9	39	3.9
k_{spa}	7.5	39	3.9
H_g	20 nm	15 nm	15 nm

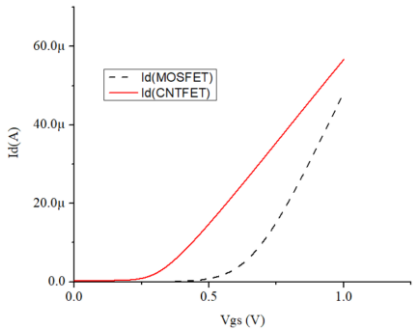
E_{fsd}	0.258	0.258	0.258
V_{fb}	0.015	0	0
Geo_mod	1	1	1
Rcmod	1	0	0
R_{s0}	3300	3300	3300
SDTmod	1	1	1
BTBTmod	1	1	1
temp	25	25	25

Chapter 4
Simulation and Analysis

The simulation result shows the different aspects of PLL when it operates in different conditions as discussed earlier when CLK_{REF} leads CLK_{FB}, then for PLL to achieve lock condition VCO output must be tuned such that the output frequency of VCO is increased. Likewise, when CLK_{REF} lags CLK_{FB}, in this scenario to operate PLL in lock condition, VCO output frequency must be decreased so that there is no phase difference between both the input signals. But before simulating the PLL block a comparison shows the I vs V characteristics of n-MOS and n-CNT FETs. All the design and simulation are performed on Cadence Virtuoso.

4.1 I-V Characteristics of n-MOSFET and N-type CNTFET

Fig. 8(a) shows the comparison of Id vs. Vgs Characteristics of nMOS and n-type CNTFET for Vds=1V, this curve shows that the drain current has a parabolic relationship with gate-to-source voltage when it exceeds the threshold point, as compared to nMOS we can see the parabolic relationship between Id and Vgs much earlier, implies that threshold voltage of nCNTFET is lower than nMOSFET. Similarly, Fig. 8(b) shows the comparison of the Id vs. Vds Characteristics of nMOS and n-type CNTFET for Vgs=1V, we can observe that the drain current saturates to a constant value once the drain-to-source voltage goes beyond the overdrive voltage i.e., (Vgs-V_{TH}) where V_{TH} is the threshold voltage, due to lower V_{TH} of CNTFETs overdrive voltage of nCNTFET is lower than the nMOSFET.



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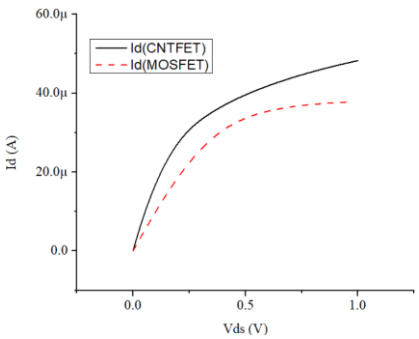
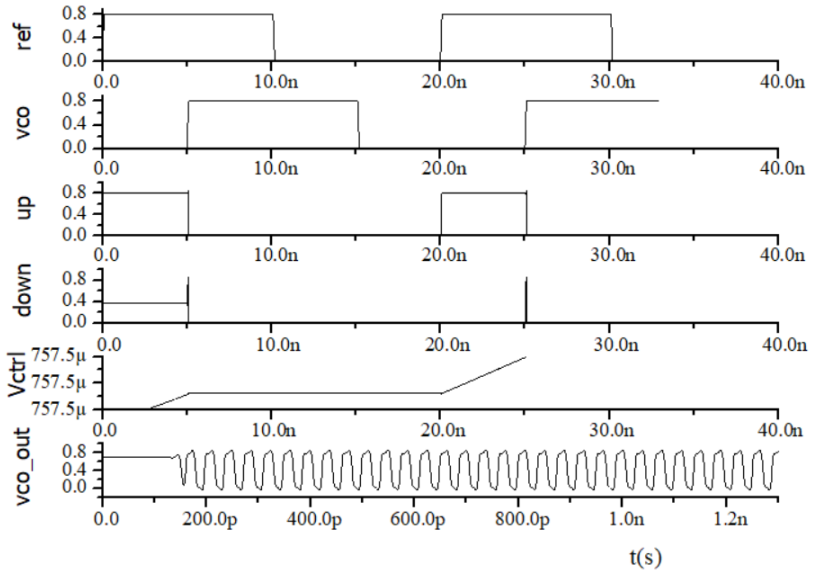


(b)

Figure 4.1 Characteristics of MOSFET and CNTFET (a) Id vs. Vgs Characteristics for Vds=1V (b) Id vs Vds Characteristics for Vgs=1V

4.2 CNTFET PLL Simulation

The simulation result shows the different scenarios of when PLL operates in different conditions as discussed earlier when CLK_{REF} leads CLK_{FB} as shown in Fig. 9(a), then for PLL to achieve lock condition VCO output must be tuned such that the output frequency of VCO is increased. Also, when CLK_{REF} lags CLK_{FB} as shown in Fig. 10(a), in this scenario to operate PLL in lock condition, VCO output frequency must be decreased so that there is no phase difference between both the input signals.



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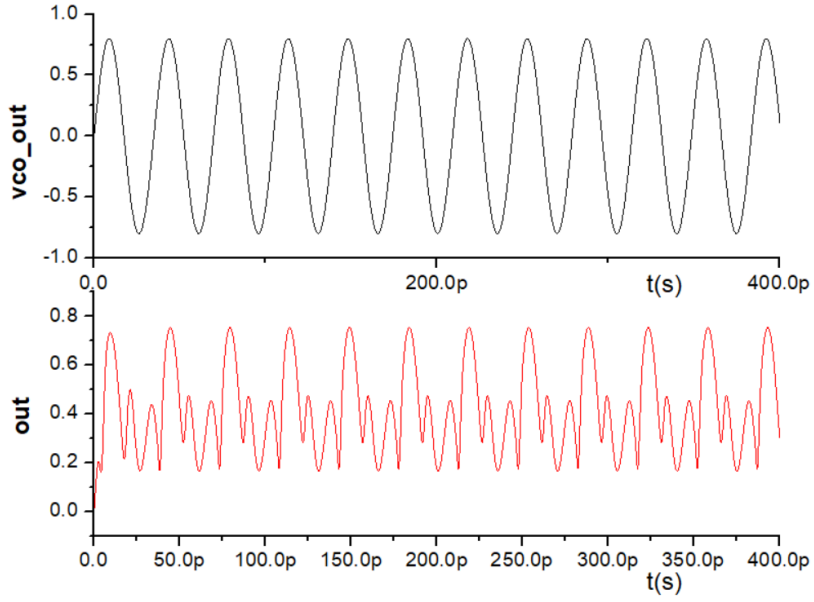
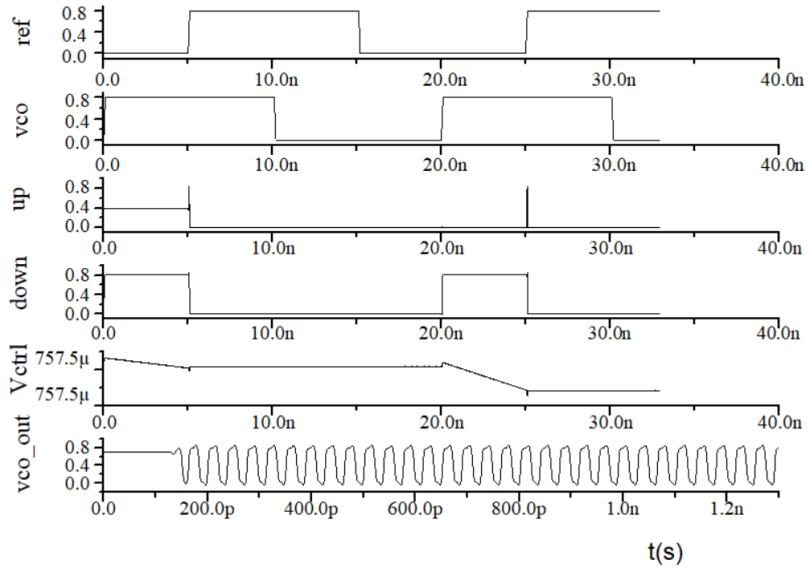
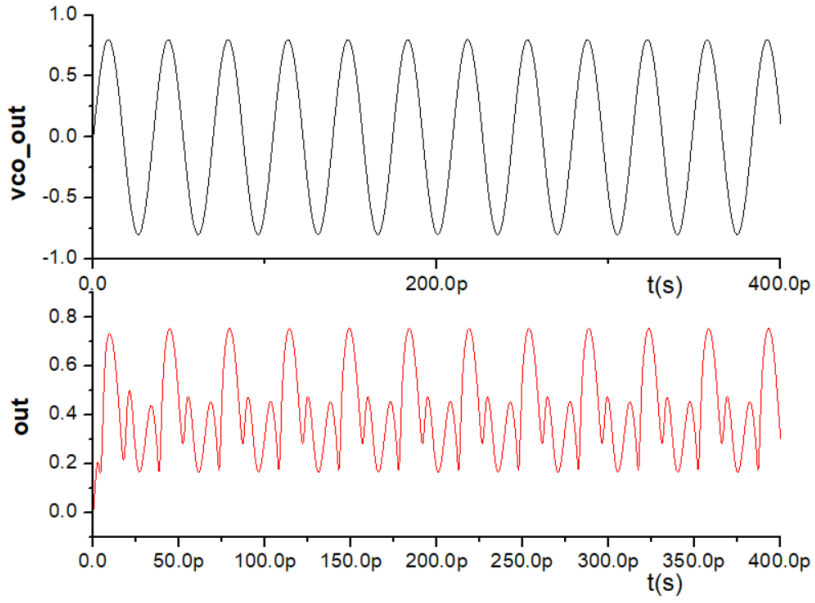


(b)

Figure 4.2.1 CNTFET PLL Output when CLK_{REF} leads (a) PLL output when CLK_{REF} leads CLK_{FB} (b) Output from frequency multiplier



(a)



(b)

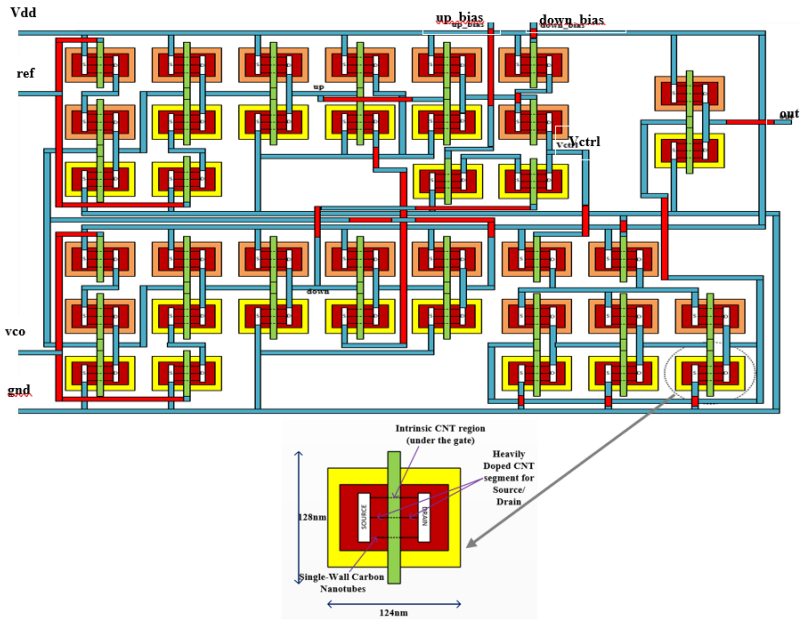
Figure 4.2.2 CNTFET PLL Output when CLK_{REF} lags (a) PLL output when CLK_{REF} lags CLK_{FB} (b) Output from frequency multiplier

4.3 Layout and Area Calculation of PLL in CNTFET Technology

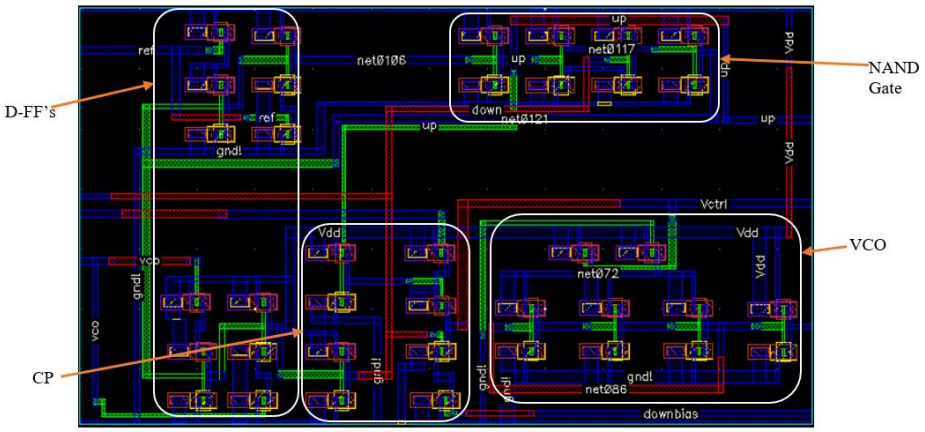
A paper by Shashikanth Bobba et al. [17], mentions that there are mainly two parameters that limit the practicality of CNTFET technology that are mispositioning or misalignment of CNTs between the terminals and the existence of metallic carbon

nanotubes in between the semiconducting carbon nanotubes when the carbon nanotubes are shifted over a substrate. Metallic CNTs are extremely unwanted as they short-circuit the drain and the source terminal of the CNTFET. Chemical etching and Electrical burning of the metallic CNTs are the main methods used so far to eliminate them from semiconducting CNTs. Zhang et al. [18] arise the practical processing strategies for metallic carbon nanotubes growth and removal.

Since design rule for any circuitry is constrained by the lithography process on it. However, there is no standard library as of now for CNTFET at 16nm of channel length it is problematic to apply state-of-the-art rules in the CNTFET technology library which is used in this design [19]. Thus, for the sake of straightforwardness and demonstration purposes, the area estimation has been done using scalable CMOS deep sub-micron rules (MOSIS) were ever needed from which the approximate active area of transistors in PLL encountered to be 3.047424e-6 mm^2 as shown in Fig. 11(a).



(a)



(b)

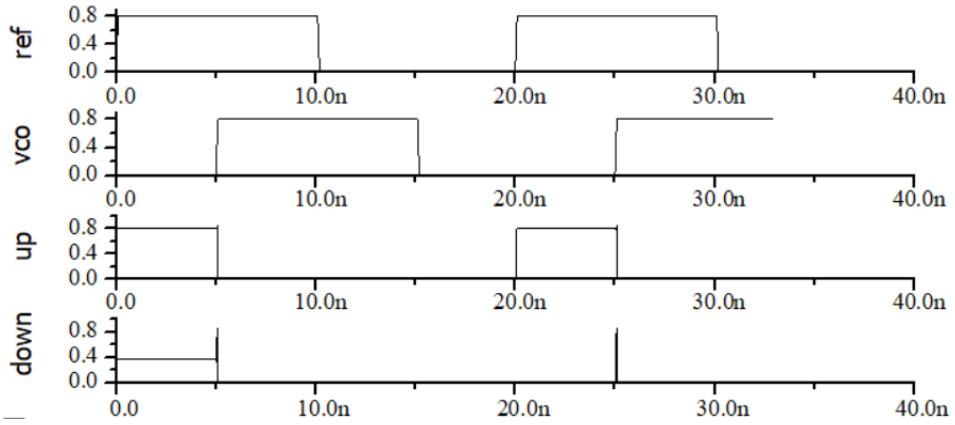
Figure 4.3 Layout of PLL (a) CNTFET PLL Layout (b) MOSFET PLL layout

Though complete IC approximate area for CNTFET is 0.46945mm^2.

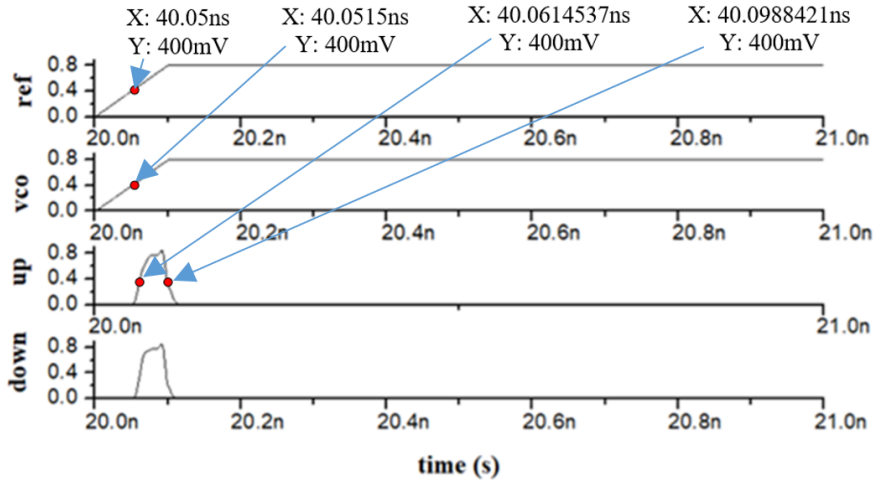
4.4 Dead Zone Analysis

The dead zone in PLL ensues when the loop doesn't respond to small phase errors between input signals of PFD or it is the maximum difference between the two input signals of PFD which cannot be detected by PFD. This problem occurs because of the delay time of both the D-FFs and the time taken by AND gate to reset D-FFs. When the two input signals are close to each other such that there is a very small phase error between both the signals then because of delay and reset time of D-FF and AND gate respectively the output signal UP and DOWN will not be able to charge and hence no output is generated. When the dead zone occurs the output signal of PFD will not be proportional to this error.

Using CNTs as the technology Fig. 12(a) shows the dead-zone free simulation of PFD and Fig. 12(b) shows the maximum phase difference which is not detected by PFD.



(a)



(b)

Figure 4.4 Dead Zone Analysis (a) PFD with no dead zone (b) PFD with dead zone

As shown in Fig. 12(b) the difference between the reference and the feedback waveforms are 1.5ps which is not detected at the output of PFD termed as dead-zone for this PFD.

4.5 Temperature Analysis

Parametric analysis is done to analyze temperature effects on CNT-based PLL. The temperature ranges from -120^{0}C to 120^{0}C, transient analysis is shown in Fig. 13. This indicates that CNTFET-based PLL can withstand temperatures from approximately -70^{0}C to 120^{0}C.

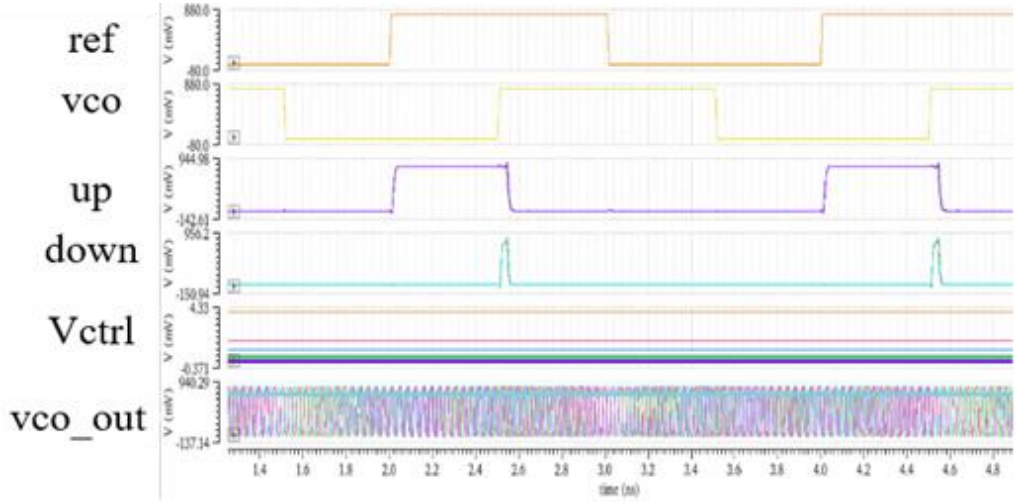


Figure 4.5 Temperature Analysis of CNT-based PLL

4.6 Comparison of Performance Parameters

Since this type of work is never done before i.e., complete design and analysis of PLL using CNTFET technology. Therefore, a comparison has been made with the MOSFET technology. As shown in Table 3, CNTFET-based PLL consumes much less power and area, and the output frequency increases as compared to MOSFETs. The drastic increases in frequency on Tan et al., [29] and this work is due to the frequency multiplier.

TABLE III
COMPARISON OF PERFORMANCE PARAMETERS WITH OTHERS WORK

Ref	Tech (nm)	Supply (V)	Output Fre. (GHz)	Area (mm^2)	Power Consumption (mW)
Meng et al., [34]	180 (CMOS)	1.8	0.24	0.078	8.46
Tseng et al., [28]	180 (CMOS)	1.2	9.953	0.9373	100

Tan et al., [29]	90 (CMOS)	1.2	76.2-89.1	1.3	62.4
Karen et al., [35]	45 (CMOS)	1.1	57-66	0.821700	78
This Work	16 (CNTFET)	0.8	86	0.46945	0.34789

Chapter 5
Discussions and Conclusion

Discussion of Results

We can hence conclude that the PLL using CNTFET occupies a less active transistor area of approximately 3.047424e-6mm^2 without the involvement of the frequency multiplier. CNTFET-based PLL consumes 18-20uW of power at 0.8V of supply voltage with an output frequency of 26.57GHz at the output of VCO which is then passed over to the frequency multiplier and we get approximately 86GHz. The dead zone is nearly 1.5ps with a reset path available to PFD. And the operating temperature range from -70°C to 120°C as shown in section 4.2.3 for the smooth working of CNTFET-based PLL. Further, the comparison was made with many technology nodes in CMOS technology because as per our research we didn't find the same work i.e., "Designing of PLL using CNTFET at deep-submicron level" to compare.

Conclusion

The PLL is used in almost every electronics device so future work can include designing frequency synthesizers, clock recovery units, etc, using CNTFET for lowering the power consumption, and area, and improving the speed of operation.

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Appendix

I. CNTFET Input Parameters Operating Range

Name	Suggested Scope	Description
type	-1 or 1	type of transistor. 1: nFET; -1: pFET
s	[2.5e-9:inf)	spacing between the CNTs (center-to-center) [m]
W	[s:inf)	transistor width [m]
L_g	[5e-9:100e-9]	physical gate length [m]
L_c	[1e-9:inf)	contact length [m]
L_{ext}	(0:inf)	source/drain extension length [m] (or spacer length)
d	[1e-9:2e-9]	CNT diameter [m]
t_{ox}	[1e-9:10e-9]	gate oxide thickness [m]
k_{ox}	[4:25]	gate oxide dielectric constant
k_{cnt}	1	CNT dielectric constant
k_{sub}	[1:kox)	substrate dielectric constant
k_{spa}	[1:16)	source/drain spacer dielectric constant
H_g	[0:inf)	gate height [m]
E_{fsd}	[-0.1:0.5]	Fermi level to the band edge [eV] at the source/drain, related to the doping density. The larger the Efsd, the higher the doping density in the source/drain extensions.
V_{fb}	[-1:1]	flat band voltage [V] (for threshold voltage adjustment)
Geomod	1 or 2 or 3	device geometry. 1: cylindrical gate-all-around; 2: top-gate with charge screening effect; 3: top-gate without charge screening effect
Rcmod	0 or 1 or 2	contact mode. 0: user-defined value, Rs0; 1: diameter-dependent transmission line model; 2: diameter-independent transmission line model (Rc is calculated at d = 1.2 nm regardless of the input d)
Rs0	[0:inf)	User-defined series resistance (Ω)
SDTmod	0 or 1 or 2	source-to-drain tunneling (SDT) mode. 0: SDT inactivated 1: SDT with inter-band tunneling 2: SDT without inter-band tunneling
BTBTmod	0 or 1	band-to-band tunneling mode. 0: off; 1: on
temp	25	Temperature (°C)